SIGNAL CONDITIONING

OUTLINE

- Introduction to signal conditioning
- Bridge circuits
- Amplifiers
- Protection
- Filters

INTRODUCTION TO SIGNAL CONDITIONING

- The output signal from the sensor of a measurement system has generally to be processed to make it suitable for the next stage of operation.
- Signal conditioning refers to operations performed on signals to convert them to a suitable for interfacing with other elements in the process-control loop.
- The signal may be:
  - Too small – have to be amplified
  - Contain interference-has to be remove
  - Non linear - required linearization
  - Be analog - have to made digital
  - Be digital – have to made analog

SIGNAL CONDITIONING

INTRODUCTION TO SIGNAL CONDITIONING

PROCESSES IN SIGNAL CONDITIONING

- The following are some of the processes that can occur in conditioning a signal.

(1) *Protection* to prevent damage to the next element

A microprocessor, as a result of high current or voltage. Thus there can be series current- limiting resistors, fuses to break if the current is too high, polarity protection and voltage limitation circuits.

(2) Getting the signal into the *right type of signal*

This can mean taking the signal into a d.c voltage or current. Thus for example, the resistance change of a strain gauge has to be converted into a voltage change. This can be done by the use of a Wheatstone bridge and using the out-of-balance voltage. It can mean taking the signal digital or analogue.

(3) Getting the *level* of the signal right

The signal from a thermocouple might be just a few milivolts. If the signal is to be fed into an analog-to-digital converter for inputting to a microprocessor then it needs to be made much larger, volts rather than milivolts. Operational amplifiers are widely used for amplification.

INTRODUCTION TO SIGNAL CONDITIONING

(4) Eliminating or reducing *noise*

Filter might be used to eliminate mains noise from a signal

(5) Signal *manipulation*

Making it a linear function of some variable. The signals from some sensors, e.g flowmeter, are non-linear and thus a signal conditioner might be used so that the signal fed on to the next element is linear

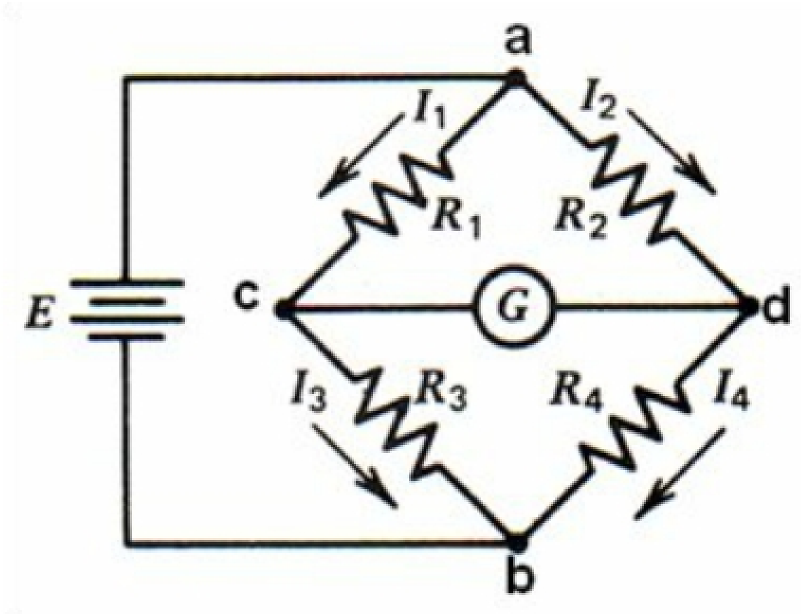
Current & voltage sensitive bridges

BRIDGE

- Bridge are electrical circuits for performing null measurements on resistances in DC and general impedances in AC.
- Bridge circuits are an integral part of measurement device. The bridges are widely used as a variable conversion element in measurement system.
- Bridge circuit are used to convert impedance variations into voltage variations. They produce an output in the form of a voltage.
- The bridge circuits operate on both null or balance condition and deflection indication principles (unbalance condition).
- Bridge can be classified into two types:
  - Direct current (dc) bridge
  - Alternating current (ac) bridge

BRIDGE CONT'D

WHEATSTONE BRIDGE



- Figure above shows the schematic diagram of a Wheatstone bridge.
- The bridge has four resistive arms together with a source of voltage and a detector meter such as galvanometer.

BALANCE CONDITION

- At balance condition, the current through the galvanometer, $I_g = 0$.
- From the previous circuit:-

At balance condition, $V_{cb} = V_{db} \rightarrow I_3R_3 = I_4R_4$ ....(1)

and, $V_{ca} = V_{da} \rightarrow I_1R_1 = I_2R_2$ ....(2)

Since the bridge is balanced, then $I_1 = I_3$; $I_2 = I_4$

Hence,

$$\boxed{\frac{V_{ca}}{V_{ca}+V_{cb}} = \frac{V_{da}}{V_{da}+V_{db}}}$$

$$\boxed{\frac{R_1}{(R_1+R_3)} = \frac{R_2}{(R_2+R_4)}}$$

Contd...

Therefore,

$$\boxed{R_1(R_2+R_4)=R_2(R_1+R_3)}$$

Thus,

$$\boxed{R_1R_4=R_2R_3}$$

$$\boxed{R_4=\frac{R_2R_3}{R_1}}$$

If R_4 is the unknown resistor, its resistance R_x can be express as follows:-

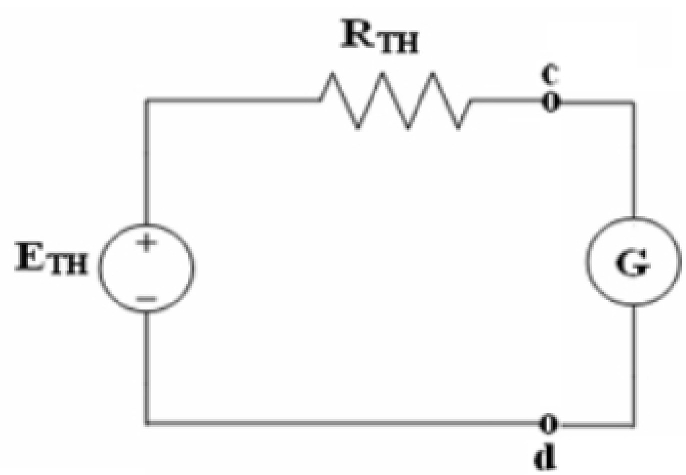
$$\boxed{R_x=\frac{R_2R_3}{R_1}}$$

BRIDGE CONT'D

- Application of balance condition Wheatstone bridge
  - It can be used to locate faults in cables
  - The principle of locating faults is the same as measuring the resistance value.
  - There are two test methods of locating the cable fault by Wheatstone bridge:
    - Murray Loop Test
    - Varley Loop Test

UNBALANCE CONDITION

- Deflection bridges are used to convert the output of resistive sensors into a voltage signal.
- When the bridge is unbalanced, there is current flowing through the galvanometer.
- The current, I_g is determine using a THEVENIN EQUIVALENT circuit Z_{TH} as figure below.



- Determination of Thevenin Equivalent circuit

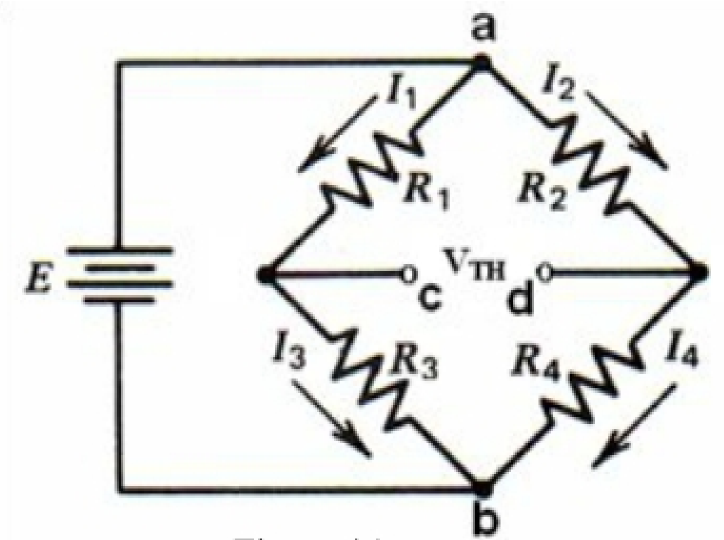


Figure (a)

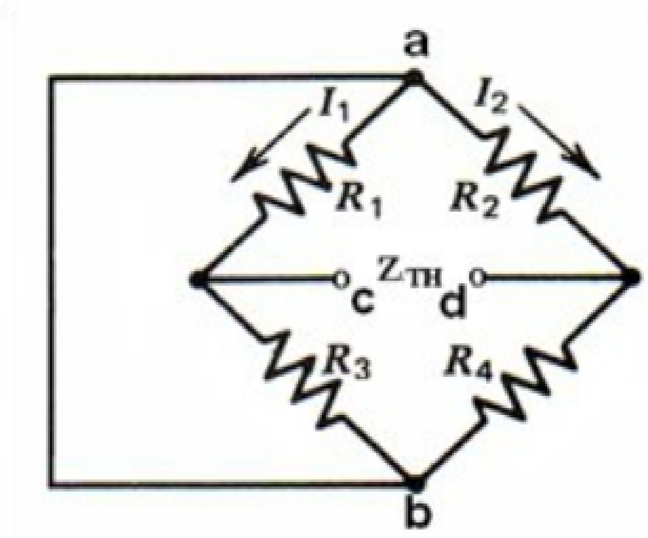


Figure (b)

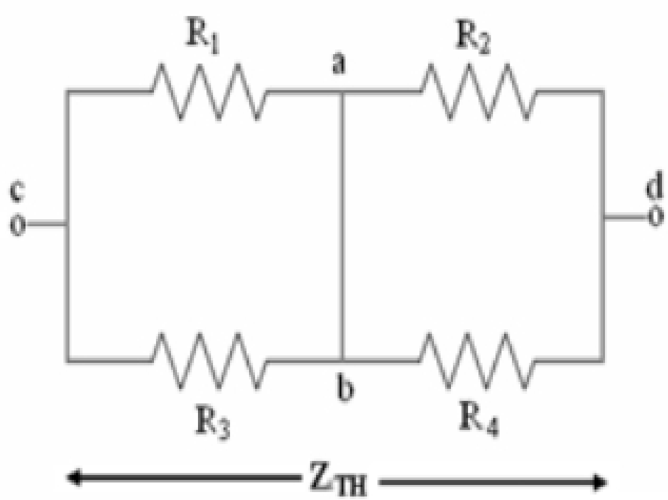


Figure (c)

BRIDGE CONT'D

Referring to Figure (a),

$$\boxed{V_{TH} = V_{cd}}$$

but

$$\boxed{V_{TH} = V_{ca} - V_{ad}}$$

$$\boxed{V_{TH} = E\left(\frac{R_1}{R_1 + R_3} - \frac{R_2}{R_2 + R_4}\right)}$$

BRIDGE CONT'D

Referring to Figure (b) and (c), Z_{TH} can be determined as follows:-

$$Z_{TH} = \frac{R_1 R_3}{R_1 + R_3} + \frac{R_2 R_4}{R_2 + R_4}$$

The Thevenin equivalent circuit is s

$$I_g = \frac{V_{TH}}{Z_{TH}}$$

Where R_g, the internal resistance of the galvanometer is neglected.

BRIDGE CONT'D

If a load is connected across the output terminals, then the current through the load is:-

$$I_g = \frac{V_{TH}}{Z_{TH} + R_G}$$

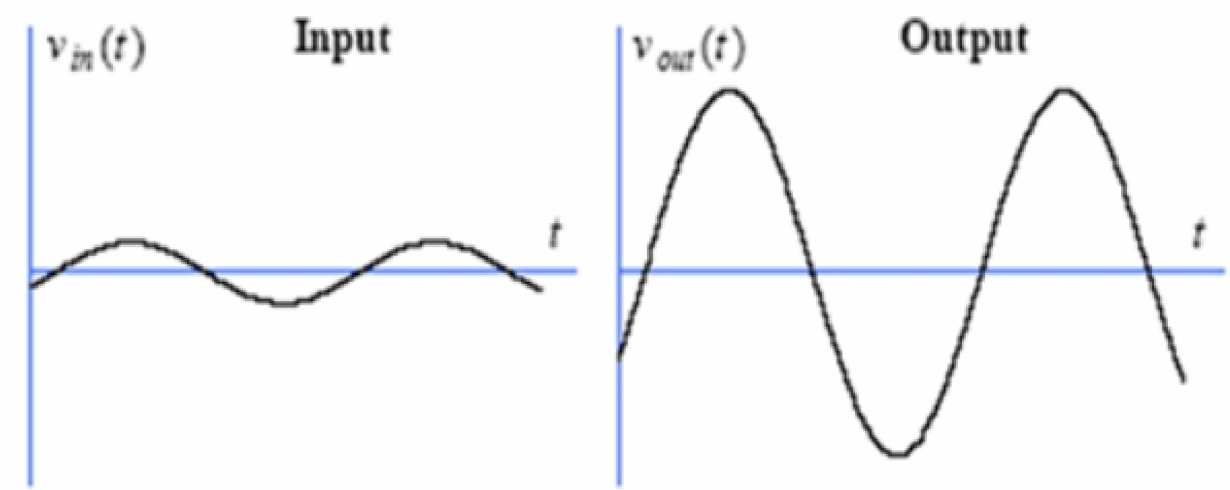
The total deflection of galvanometer can be determined as:

$$D = SI_g$$

Where S is the sensitivity of galvanometer in unit mm/μA

AMPLIFIER

An amplifier is an electronic circuit which makes a signal bigger.



Amplification is often needed in systems using analogue signals.

Explain the concept of Signal Conditioning

PROTECTION

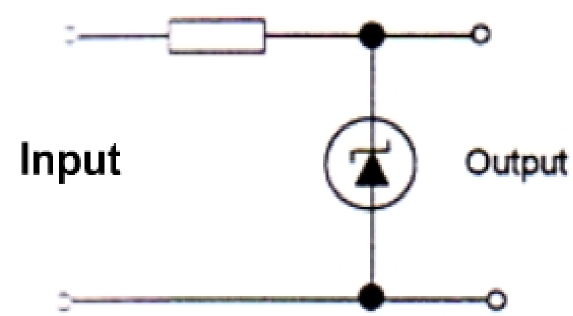
Problem

A unit after a sensor has a possibility of damage by high current or high voltage

How to protect?

High Current	High Voltage
a series resistor to limit the current to an acceptable level a fuse to break if the current does exceed a safe level.	the use of a Zener diode circuit

PROTECTION CONT'D



Zener diodes behave like ordinary diodes up to some breakdown voltage when they become conducting.

Thus to allow a maximum voltage of 5 V but stop voltages above 5.1 V getting through, a Zener diode with a voltage rating of 5.1 V might be chosen.

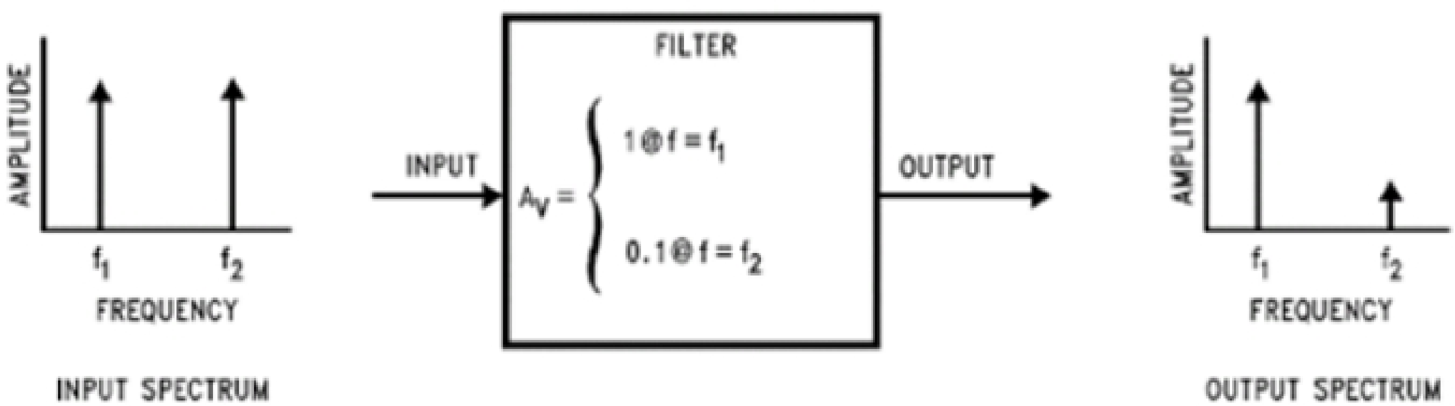
When the voltage rises to 5.1 V the Zener diode breakdown and its resistance drops to a very low value.

The result is that the voltage across the diode, and hence that outputted to the next circuit, drops.

Because the Zener diode is a diode with a low resistance for current in one direction through it and a high resistance for the opposite direction.

FILTER

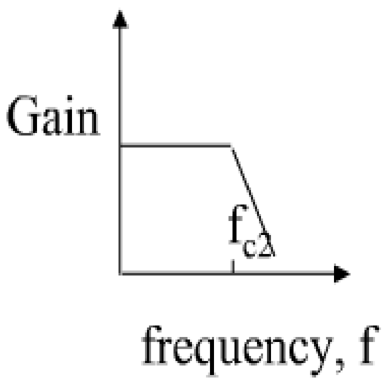
- WHAT DOES A FILTER DO?
  - In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency.
  - Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges/decrease the amplitude.



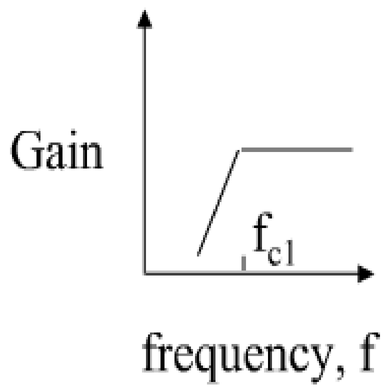
FILTER CONT'D

- Elimination / reduction of noise: electromagnetic (EM), mains, vibration etc.
- Detection of particular signal frequencies.

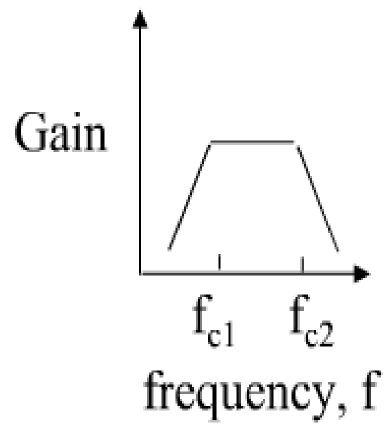
Low pass filter



High pass filter

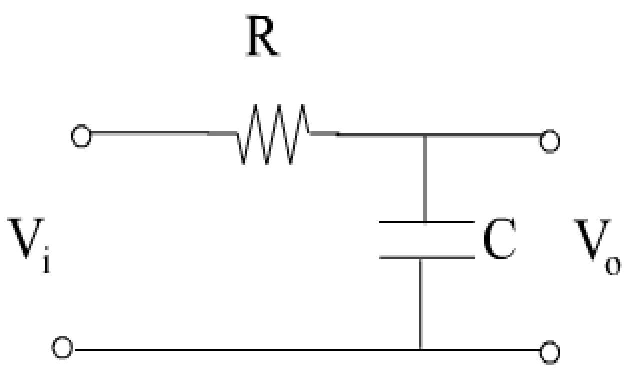


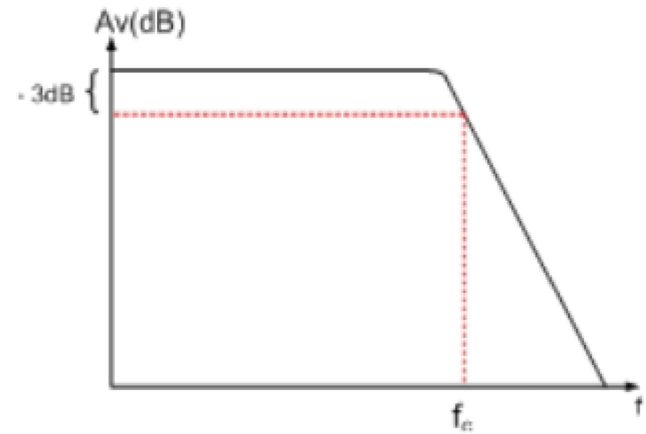
Band pass filter



FILTER CONT'D

LOW PASS FILTER

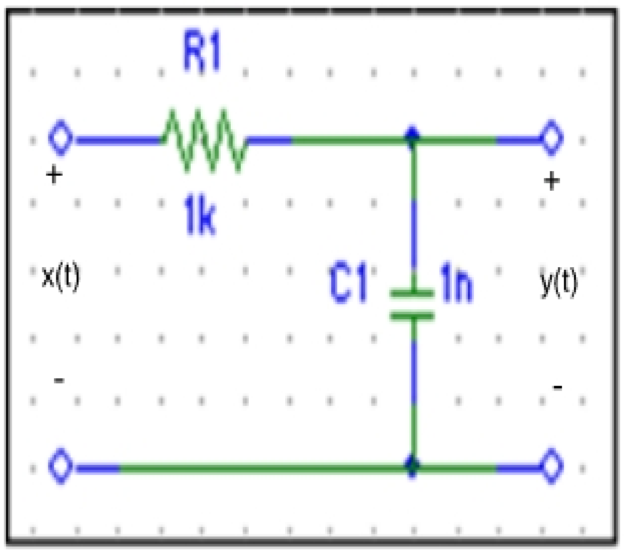


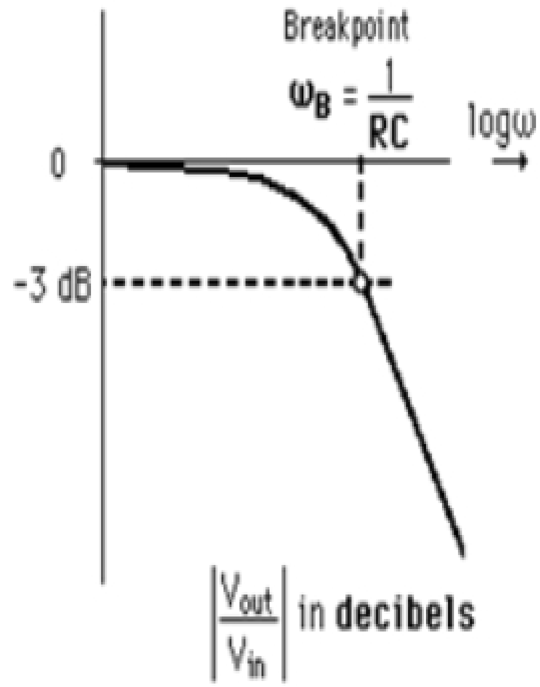


- A filter designed to pass all frequency below a given cut-off frequency
- Approximate low frequency with $w \rightarrow 0$ and high frequency with $w \rightarrow \infty$
  - at low frequency, gain = 1, &
  - at high frequency, gain = 0

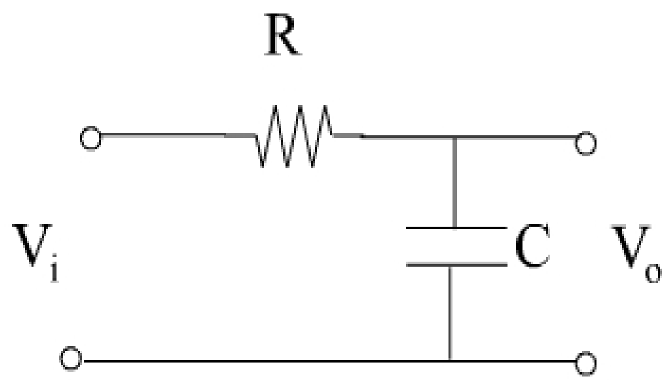
FILTER CONT'D

Low-pass Filter





FILTER CONT'D



$$V_o = \frac{1}{1 + j\omega RC} V_i$$

$$\text{gain} = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

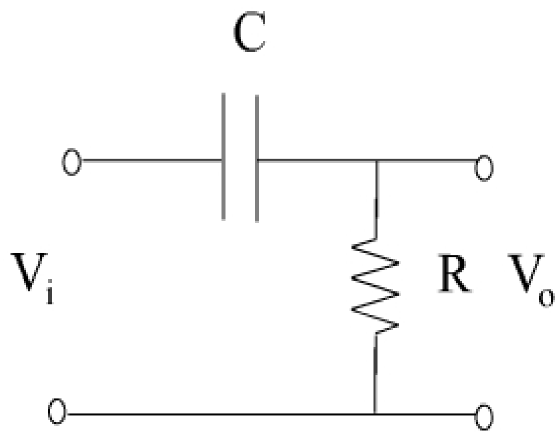
Cut off frequency is where the gain = $1/\sqrt{2}$ (= –3 dB)

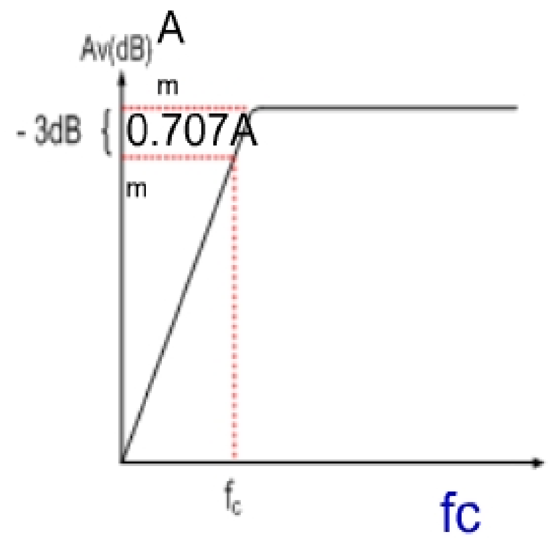
At cut-off frequency $Z_R = Z_c$. Therefore

$$\boxed{f_c = 1/(2\pi RC)}$$

FILTER CONT'D

HIGH PASS FILTER

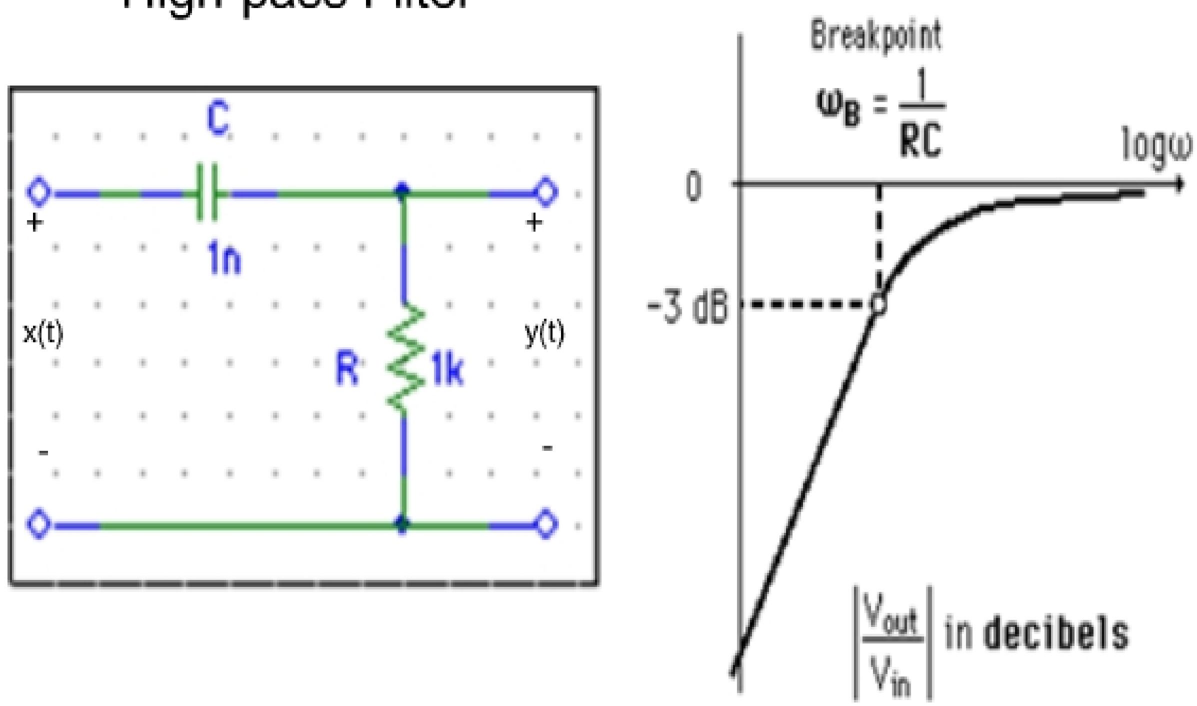




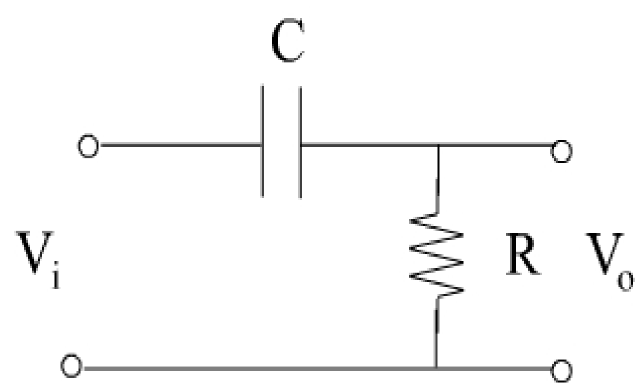
- A filter designed to pass all frequency above a given cut-off frequency
- Approximate low frequency with w → 0 and high frequency with w → ∞
  - at low frequency, gain = 0, &
  - at high frequency, gain = 1

FILTER CONT'D

High-pass Filter



FILTER CONT'D



$$V_o = \frac{j\omega RC}{1 + j\omega RC} V_i$$

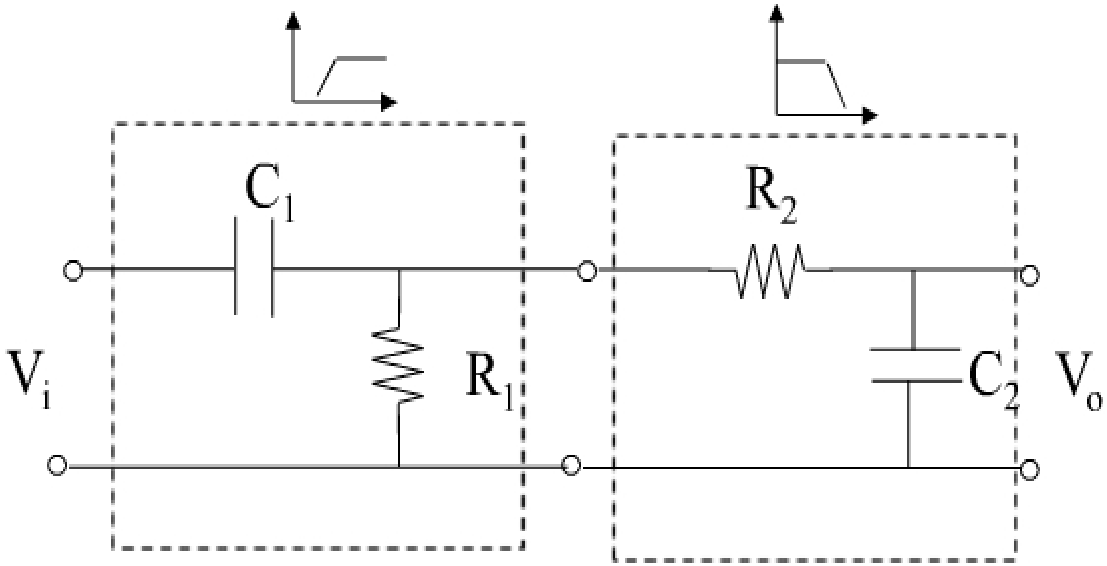
$$\text{gain} = \left|\frac{V_o}{V_i}\right| = \frac{\omega RC}{\sqrt{1+(\omega RC)^2}}$$

Cut off frequency is where the gain = $1/\sqrt{2}$ (= –3 dB)

At cut-off frequency $Z_R = Z_c$. Therefore

$$\boxed{f_c = 1/(2\pi RC)}$$

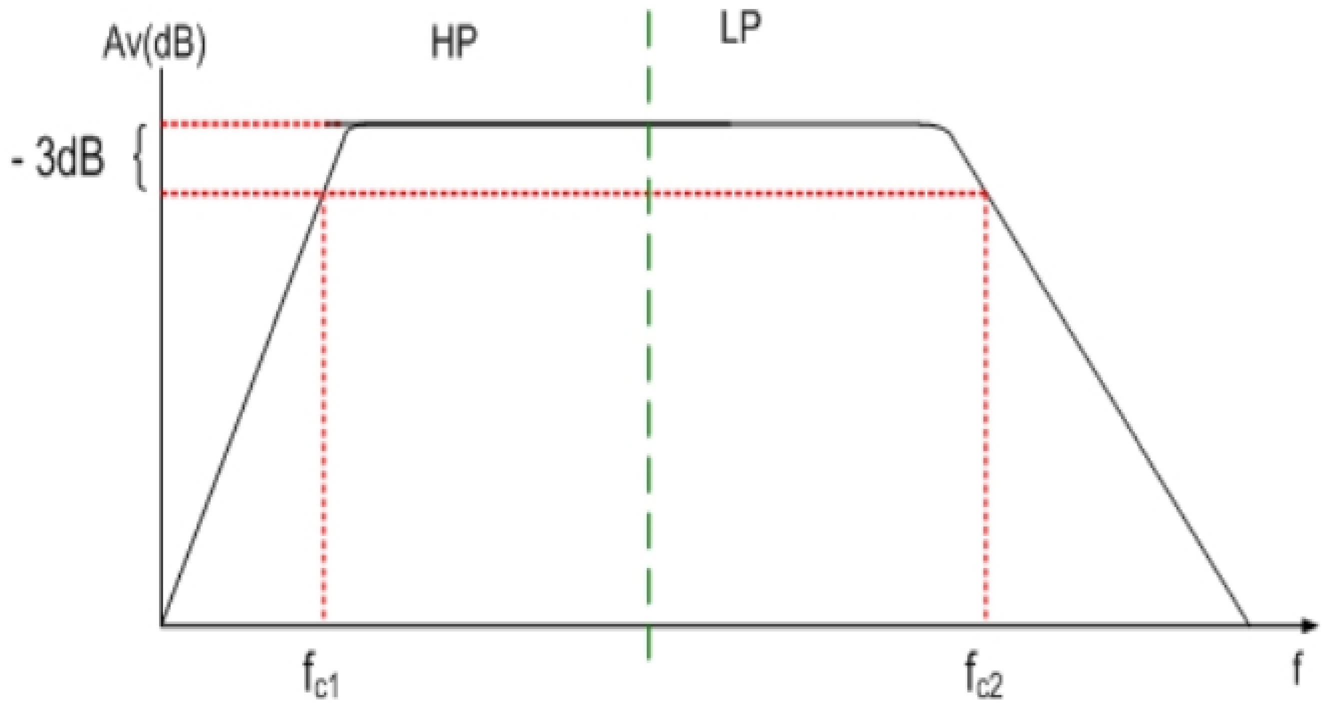
BAND PASS FILTER



- Designed to pass all frequency that fall between fc1 and fc2
- High pass filter followed by Low pass filter
- Gain :

$$\left|\frac{V_o}{V_i}\right| = \frac{\omega R_1 C_1}{\sqrt{1+(\omega R_1 C_1)^2}} \frac{1}{\sqrt{1+(\omega R_2 C_2)^2}}, \quad f_{c1} = \frac{1}{2\pi R_1 C_1} < \frac{1}{2\pi R_2 C_2} = f_{c2}$$

FILTER CONT'D



FILTER CONT'D

LP

$$\boxed{V_o = \frac{Z_c}{Z_c + Z_R}(V_i)}$$

$$\frac{V_o}{V_i} = \frac{Z_c}{Z_c + Z_R}$$

$$= \frac{1/j\omega C}{1/j\omega C + R}$$

$$= \frac{\left(\frac{1}{j\omega C}\right)}{\left(\frac{1 + j\omega RC}{j\omega C}\right)}$$

$$= \frac{1}{1 + j\omega RC}$$

$$\boxed{\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}}$$

HP

$$\boxed{V_o = \frac{Z_R}{Z_c + Z_R}(V_i)}$$

$$\frac{V_o}{V_i} = \frac{Z_R}{Z_c + Z_R}$$

$$= \frac{R}{1/j\omega C + R}$$

$$= \frac{R}{\left(\frac{1 + j\omega RC}{j\omega C}\right)}$$

$$= \frac{j\omega RC}{1 + j\omega RC} \approx \frac{0 + j\omega RC}{1 + j\omega RC}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{\sqrt{0^2 + (\omega RC)^2}}{\sqrt{1 + (\omega RC)^2}}$$

$$\boxed{\left|\frac{V_o}{V_i}\right| = \frac{\omega RC}{\sqrt{1 + (\omega RC)^2}}}$$

Asssignment

- Explain the working of high and low pass filter

Shielding and Grounding

Characteristics of Electrical Noise

- Noise definition
  - A stochastic interfering or modifying input (not the desired signal) in a system.
  - Types
    - Classification
      - Source - man-made / natural
      - Bandwidth – narrow / broadband
      - Coherency (has phase and frequency consistency)
      - Reception mode – radiated or conducted
    - Inherent - generated within the elements of a circuit or system
      - Examples
        - thermal noise (Johnson noise)
        - Current related junction noise (Shot noise)
    - Interference - Generated external to the circuit or system
      - Examples might be EMI (electromagnetic interference) from a radio station

Characterization of Noise

- Signal to noise ratio

$$SNR_{db} = 10\log\left(\frac{Signal\ Power}{Noise\ Power}\right)$$

$$SNR_{db} = 10\log\left(\frac{\dfrac{V_{signal}^2}{Z_{load}}}{\dfrac{V_{noise}^2}{Z_{load}}}\right) = 10\log\left(\frac{V_{signal}^2}{V_{noise}^2}\right) = 20\log\left(\frac{V_{signal}}{V_{noise}}\right)$$

- Noise Figure – for an amplifier circuit

$$10\log\left(\frac{SNR_{out}}{SNR_{in}}\right)$$

Noise terminology

- The noise voltage
  - *Equivalent short-circuit input RMS noise voltage*
    - *The apparent noise voltage at the input of the noiseless amplifier with a shorted input*
    - *nV per √Hz or nV in a given frequency band*
- . The noise current
  - *Equivalent short-circuit input RMS noise current*
    - *The apparent noise current at the input of the noiseless amplifier due only to noise currents*
    - *nA per √Hz or nA in a given frequency band*

Inherent noise

- Generated within or by the device in question
- Types
  - Thermal Noise - Johnson noise
    - Function of thermally induced electron motion
    - Gaussian amplitude distribution (white).
    - Independent of direct-current flow.
    - Calculated as Equation ~~4.88 in Fraden (Johnson~~, 1928)

$$V_{thermal} = \sqrt{4 \cdot 1.38 \times 10^{23} TR\Delta f} \quad \left[V / \sqrt{Hz}\right]$$

    - Noise power (V^2) is proportional to resistance (R), temperature (T), and bandwidth Δf
    - Estimated for resistances as:
    - Reduction of thermal noise for fixed R:
      - lower component temperature
      - minimize bandwidth

$$V_{thermal} \approx 0.13\sqrt{R}\left(\sqrt{\Delta f}\right) \quad [nV]$$

Inherent Noise - continued

- Types - continued
  - Shot Noise - Current related noise in semi-conductors
    - Proportional to junction current in a semiconductor
      - Example: The higher the bias current on a photodiode, the higher the shot noise will be.
    - Calculation: $$i_{shot} = \sqrt{2 q i_{dc} \Delta f}$$
    - Caused by random arrival times of electrons in a current flow across a junction.
    - Always associated with a direct-current flow.
    - Proportional to the electronic charge and current.
    - Gaussian amplitude distribution (white).
    - Reduction of shot noise
      - decrease currents
      - design for narrow bandwidth

Inherent Noise - continued

- Types - continued
  - Pink Noise or 1/f Noise or flicker noise
    - Noise that increases in magnitude with 1/f
    - Associated with conduction
      - Significant in semi-conductors, carbon film resistors, diodes, transistors, and light sources
    - Associated with Flows of carriers in a discontinuous medium
      - Contamination during manufacture increases this noise
    - Dominates thermal noise below 100 hz
    - Calculation:
    - Reduction of 1/f noise
      - Reduce current
      - Design for narrow bandwidth
      - Use high quality components

$$i_{flicker} = \sqrt{K\left(\frac{i_{dc}}{f}\right)^{a}\Delta f}$$

K = constant for a particular device
I = direct current
a = constant in range 0.5 to 2
b= constant about unity
Δf=small bandwidth at frequency f

Minimization of inherent noise

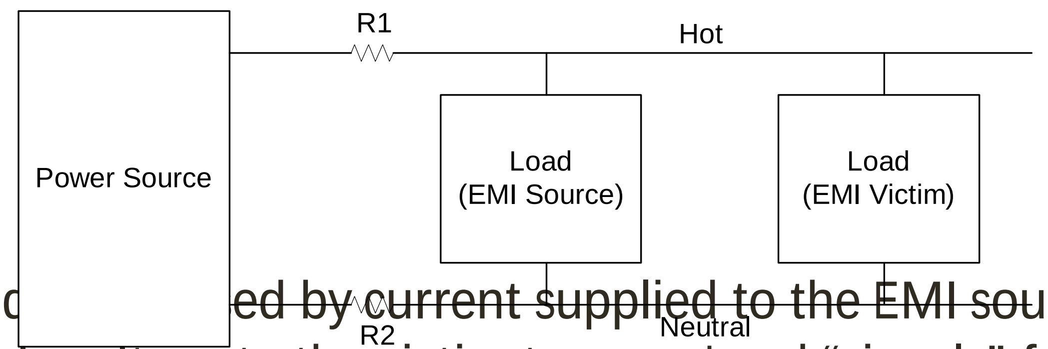
- Operate circuits at low current levels
  - Choose low-power technology CMOS, etc.
  - Use low power op-amps
- Eliminate use of carbon film resistors in critical areas
  - (carbon film has high 1/f noise)
- Operate circuits at low temperature
  - Use cooling devices (note, thermal noise is proportional to absolute temperature)
- Purchase modern better quality components
- Design to use narrowest possible bandwidth

EMI - ElectroMagnetic Interference

- EMI - Noise that is coupled into a system from external sources.
- Types (Coupling mechanisms)
  - Galvanic coupling (Conductive coupling)
  - Magnetic induction (inductive coupling)
  - Electric induction - (capacitive coupling)

Conducted EMC

- Conductive or galvanic connection
  - Interference due to voltage drops in power and signal conductors.
  - Example: Through the power line or “mains”



  - Voltage d[illegible]ed by current supplied to the EMI source load causes the supply voltage to the victim to vary. Load “signals” from the source are applied directly to the victims power supply.
  - May occur in situations other than power distribution

Reduction of conducted EMI

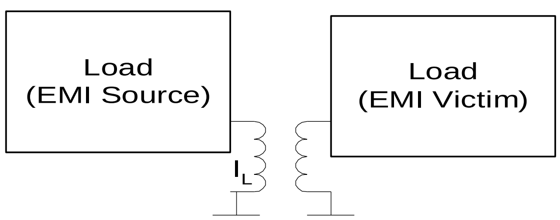
- Reduction of galvanic coupled interference
  - minimize parallel connected systems
  - Use capacitive de-coupling of the power supply for each component in parallel connected power distribution
  - assure adequate capacity of conductors in parallel connected power distribution
  - reduce power consumption

Inductively coupled EMI

- Magnetic induction (inductive coupling)
  - Coupling of source signals to victim system through a magnetic field. This effect occurs as a result of mutual inductance.

$$e_m = -M \frac{di_L}{dt}$$

  - where M = mutual inductance between source and victim
  - i_L = load side current of the inductive coupling

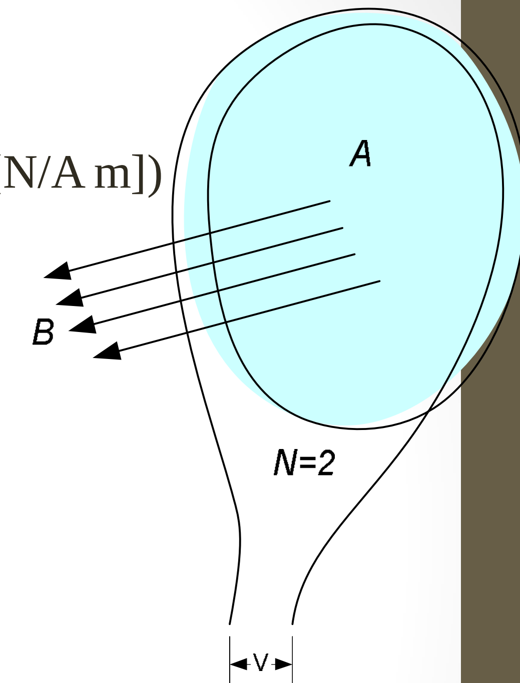


  - M = function of loop areas, loop orientations, magnetic screening

Inductive coupling: Analysis through Faraday's Law

$$V = -N\frac{d\phi}{dt} = \frac{d(BA)}{dt}$$

B = Magnetic field [T] (or [N/A m])
A = area of coil [m^2]
t = time [s]
V = voltage [v]
N = number of turns of coil



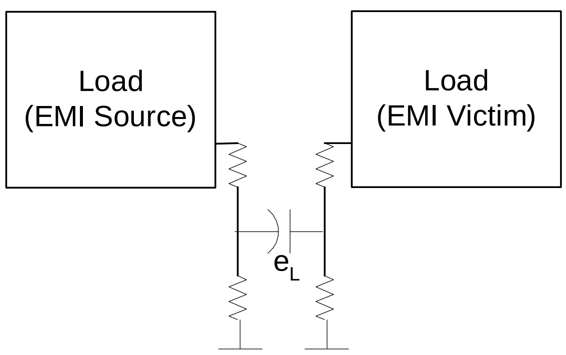
- Reduction of inductively coupled EMI:
  - Minimize area (rate of change of area)
  - Minimize magnetic field (rate of change of magnitude and direction)
  - Minimize number of turns (inductance)
- Common methods
  - Use twisted pair wiring
  - Use magnetic shielding
  - Run conductor pairs close together on circuit boards

Capacitively coupled EMI

- Electric induction - (capacitive coupling)
  - Coupling of source signals to victim system through an electric field. This effect occurs as a result of a capacitive coupling.

$$i_c = C_c \frac{de_L}{dt} \qquad C_c = \frac{k\varepsilon_0 A}{d}$$

  - Where C_c is the capacitance of the coupling between source and victim and e_L is the voltage drop between source and victim across the coupling.

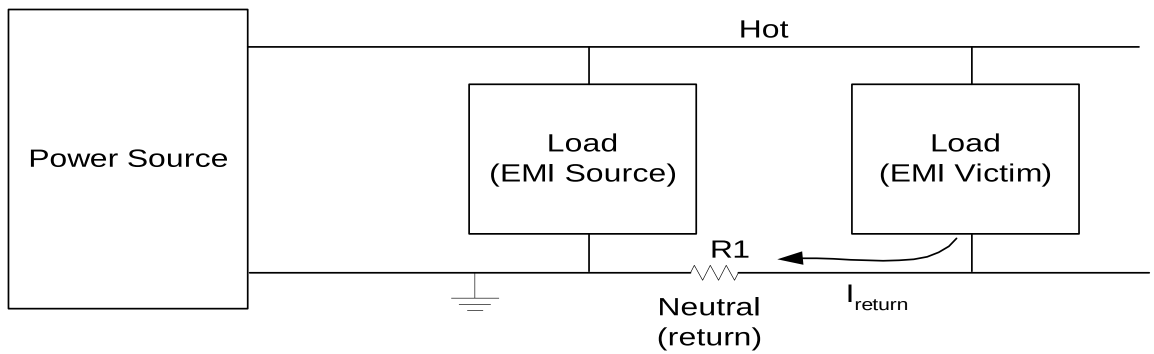


Reduction of capacitively coupled EMI

- Reduction of capacitively coupled EMI
  - Reduce capacitance of coupling
    - Cc depends on separation distance between “plates”, plate area, dielectric permittivity of the capacitor’s medium
    - Increase plate separation
    - Decrease plate area
    - Decrease voltage level of source
  - Common methods
    - Separate victim circuit from EMI source
    - Provide a conductive shield at low potential around victim and or source

Grounding Issues

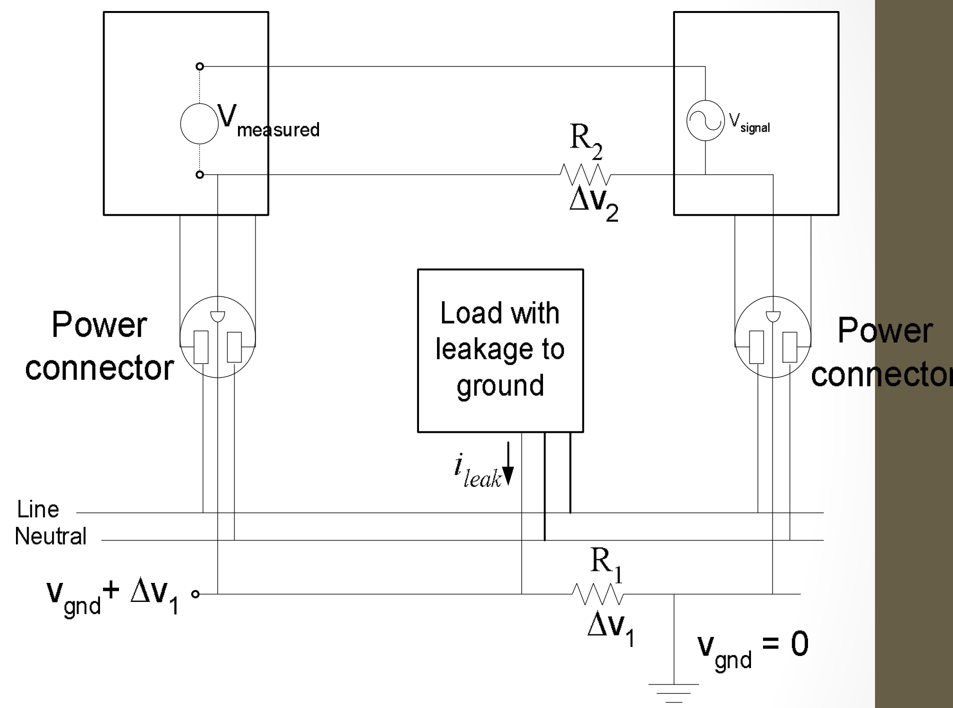
- Differences in “ground” level in systems can be an inherent source of interference.



  - Voltage drop in the return across R1 causes signals from the source to appear to have a component of the power line current from the point of view of the victim
  - Any duplicate low impedance ground path (ground loop) will have high current

Ground loop example

- Consider a typical situation:
  - Leakage to the ground conductor in a system outside the measuring system
  - Resistance between the load and the system ground
  - Power connections in the system of interest at different locations

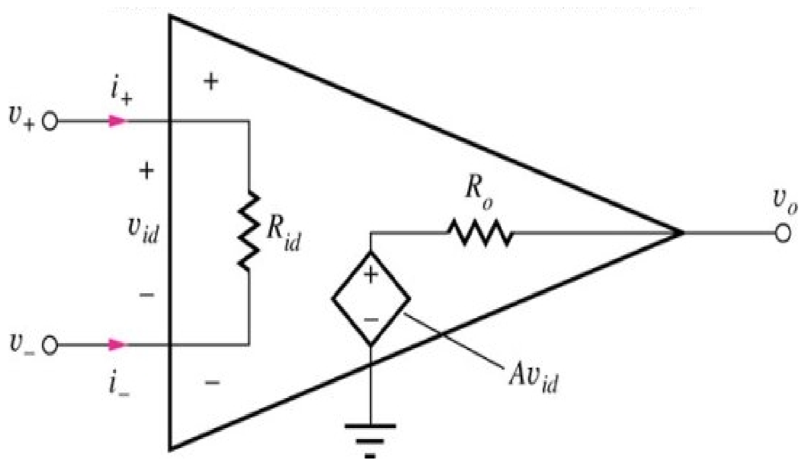


Assignment

- Explain the advantages of Shielding & grounding and its concept

Operational Amplifiers

Differential Amplifier Model: Basic



Represented by:

A = open-circuit voltage gain

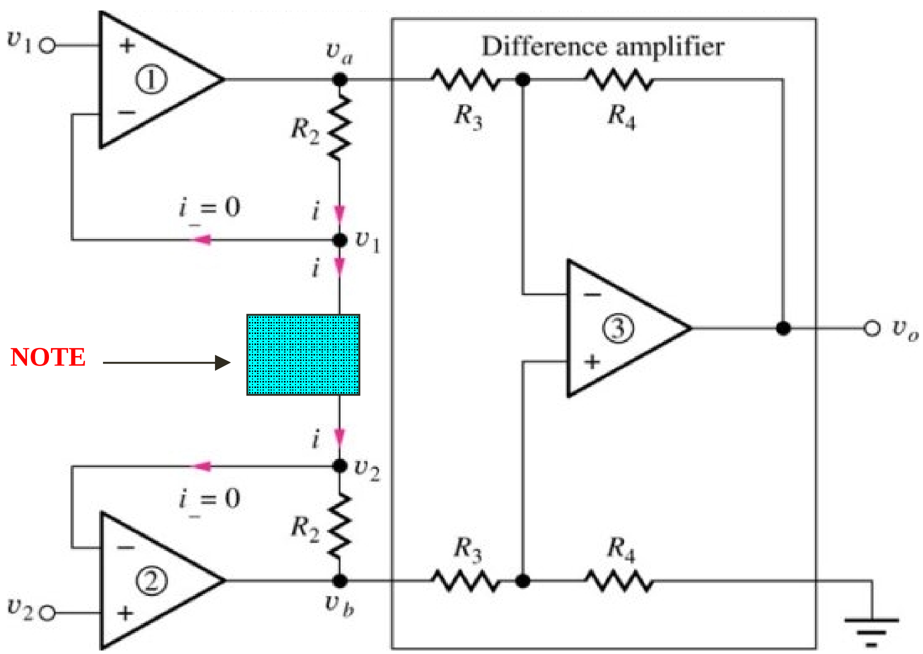
v_{id} = (v^+-v^-) = differential input signal voltage

R_{id} = amplifier input resistance

R_o = amplifier output resistance

The signal developed at the amplifier output is in phase with the voltage applied at the + input (non-inverting) terminal and 180° out of phase with that applied at the - input (inverting) terminal.

Instrumentation Amplifier



$$v_o = -\frac{R_4}{R_3}(v_a - v_b)$$

$$v_a - iR_2 - i(2R_1) - iR_2 = v_b$$

$$i = \frac{v_1 - v_2}{2R_1}$$

$$\therefore v_o = -\frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)(v_1 - v_2)$$

Combines 2 non-inverting amplifiers with the difference amplifier to provide higher gain and higher input resistance.

Ideal input resistance is infinite because input current to both op amps is zero. The CMRR is determined only by Op Amp 3.

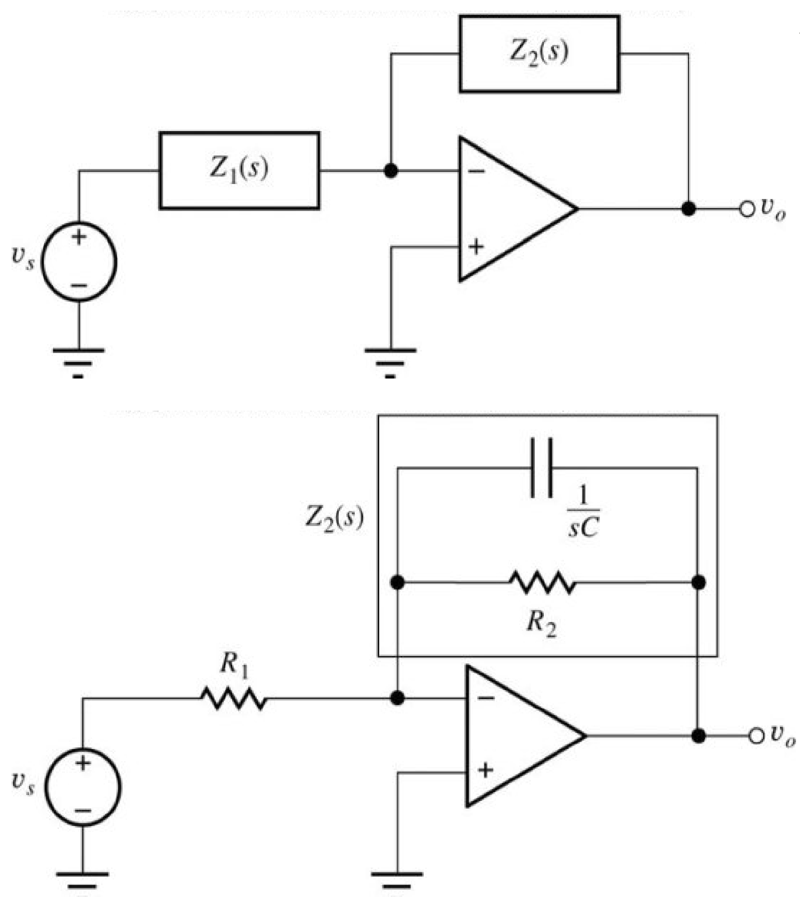
Instrumentation Amplifier: Example

- **Problem**: Determine V_o
- **Given Data**: $R_1 = 15\ \text{k}\Omega$, $R_2 = 150\ \text{k}\Omega$, $R_3 = 15\ \text{k}\Omega$, $R_4 = 30\ \text{k}\Omega$ $V_1 = 2.5$ V, $V_2 = 2.25$ V
- **Assumptions:** Ideal op amp. Hence, $v_- = v_+$ and $i_- = i_+ = 0$.
- **Analysis:** Using dc values,

$$A_{dm} = -\frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right) = -\frac{30\text{k}\Omega}{15\text{k}\Omega}\left(1+\frac{150\text{k}\Omega}{15\text{k}\Omega}\right) = -22$$

$$V_o = A_{dm}(V_1 - V_2) = -22(2.5-2.25) = -5.50\text{V}$$

The Active Low-pass Filter



Use a phasor approach to gain analysis of this inverting amplifier. Let s = jω.

$$A_v = \frac{\tilde{v}_o(j\omega)}{\tilde{v}(j\omega)} = -\frac{Z_2(j\omega)}{Z_1(j\omega)} \qquad Z_1(j\omega) = R_1$$

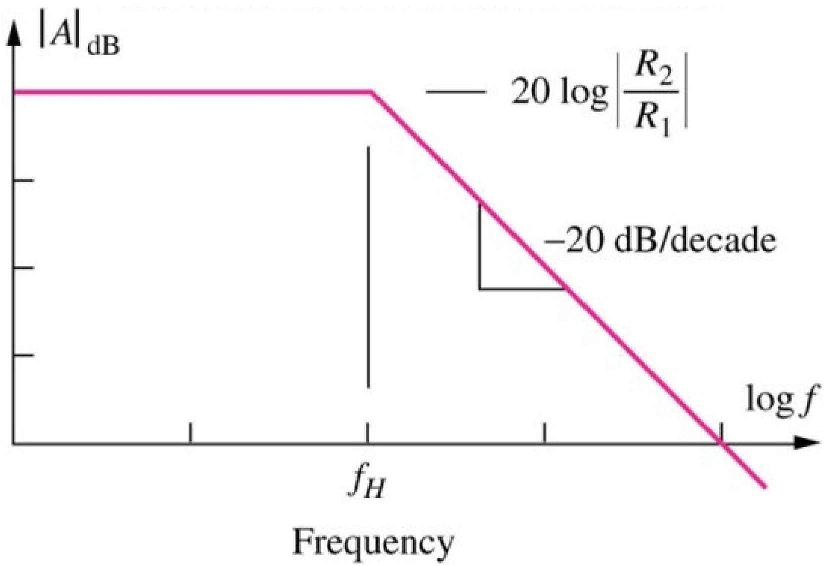
$$Z_2(j\omega) = \frac{R_2 \dfrac{1}{j\omega C}}{R_2 + \dfrac{1}{j\omega C}} = \frac{R_2}{j\omega C R_2 + 1}$$

$$A_v = -\frac{R_2}{R_1}\frac{1}{(1 + j\omega C R_2)} = \frac{R_2}{R_1}\frac{e^{j\pi}}{(1 + \dfrac{j\omega}{\omega_c})}$$

$$\omega_c = 2\pi f_c = \frac{1}{R_2 C} \quad \therefore f_c = \frac{1}{2\pi R_2 C}$$

f_c is called the high frequency “cutoff” of the low-pass filter.

Active Low-pass Filter (continued)



- At frequencies below f_c (f_H in the figure), the amplifier is an inverting amplifier with gain set by the ratio of resistors R_2 and R_1.
- At frequencies above f_c, the amplifier response "rolls off" at -20dB/decade.
- Notice that cutoff frequency and gain can be independently set.

$$A_v = \frac{R_2}{R_1}\left(\frac{e^{j\pi}}{(1+\frac{j\omega}{\omega_c})}\right) = \frac{R_2}{R_1\sqrt{1^2+\left(\frac{\omega}{\omega_c}\right)^2}}\left(\frac{e^{j\pi}}{e^{j\tan^{-1}(\omega/\omega_c)}}\right) = \underbrace{\frac{R_2}{R_1\sqrt{1+\left(\frac{\omega}{\omega_c}\right)^2}}}_{\text{magnitude}}\, e^{\overbrace{j[\pi-\tan^{-1}(\omega/\omega_c)]}^{\text{phase}}}$$

Analog to Digital (AD), Digital to Analog (DA) conversion

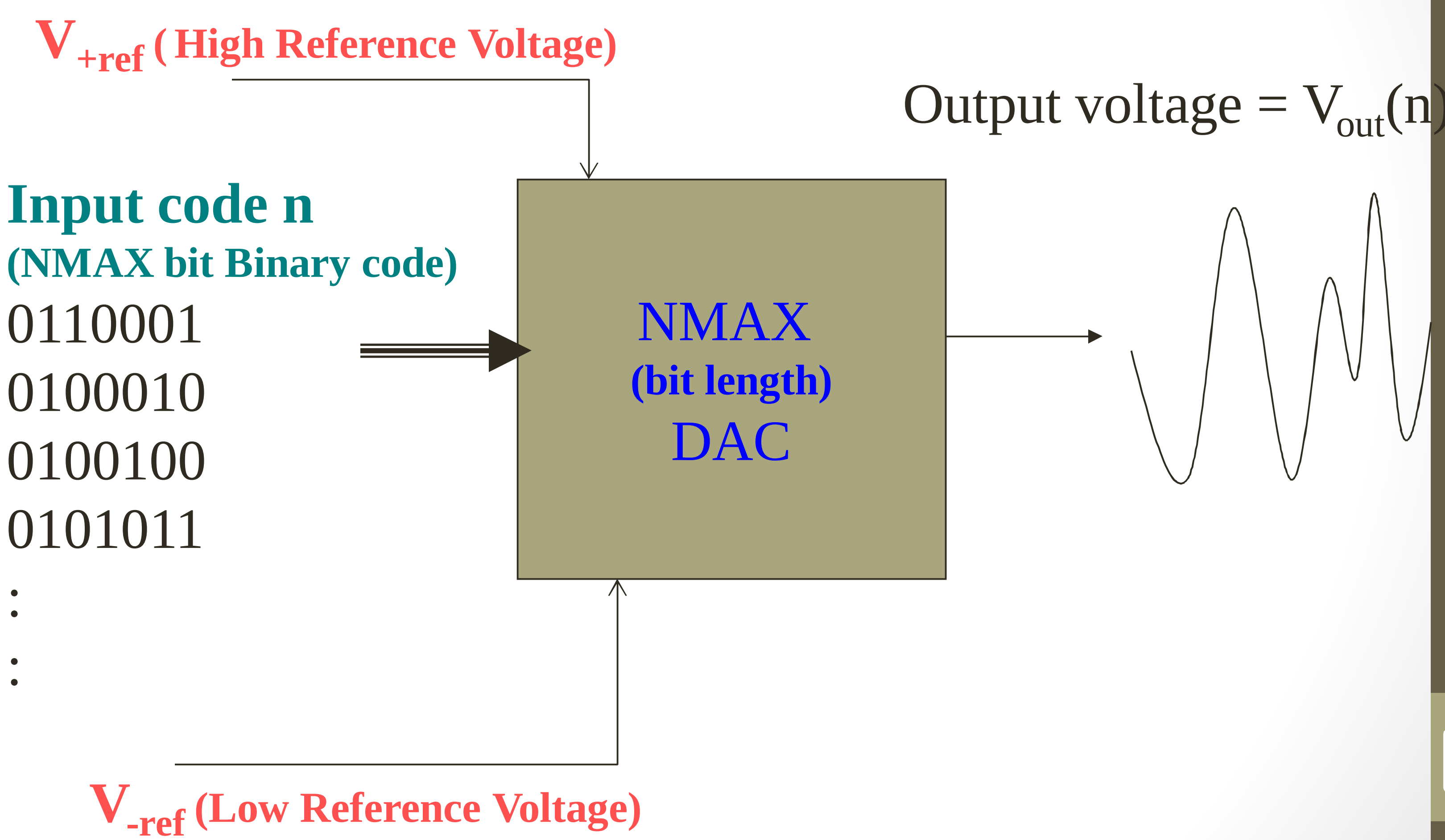
Analog/digital conversions

- Topics
  - Digital to analog conversion
  - Analog to digital conversion
  - Sampling-speed limitation
  - Frequency aliasing
  - Practical ADCs of different speed

Digital to Analogue Conversion

DAC

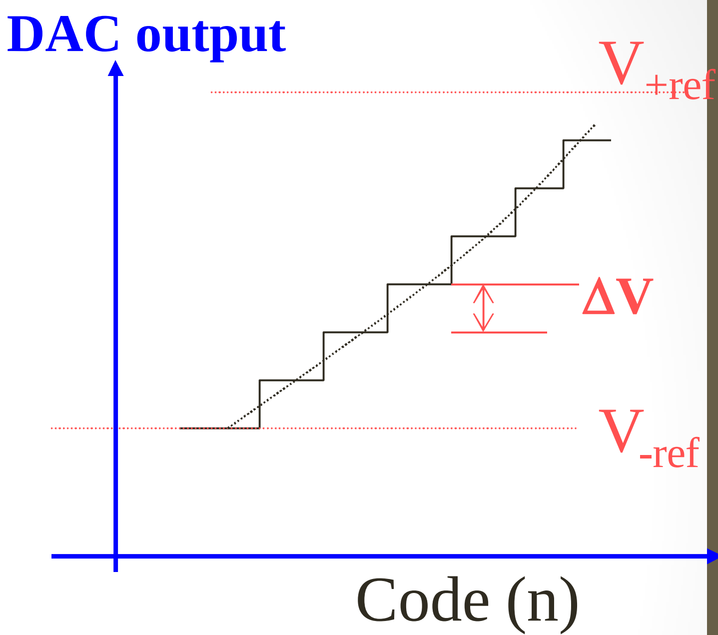
Digital to analog converter (DAC)



DAC: basic equation

$$V_{out}(n) = V_{-ref} + n\left[\frac{V_{+ref} - V_{-ref}}{2^{NMAX}}\right]$$

$$= V_{-ref} + n\Delta V$$



- At $n=0$, $V_{out}(0) = V_{-ref}$
- At max. $n\_max = 2^{NMAX} - 1$,
- (E.g. NMAX=8, n_max=2^8-1=255)
  - V_{out} cannot reach V_{+ref} ,
  - E.g. NMAX=8, n=0, 1, 2, ... 255.
- Some DACs have internal reference voltage settings, some can be set externally.

DAC: characteristics

- Glitch: A transient spike in the output of a DAC that occurs when more than one bit changes in the input code.
  - Use a low pass filter to reduce the glitch
  - Use sample and hold circuit to reduce the glitch
- Settling time: Time for the output to settle to typically 1/4 LSB after a change in DA output.

Two DAC implementations

- Type 1: Weighted Adder DAC
  - Easy to design, use many different Resistor values so it is difficult to manufacture.
- Type 2: R-2R Resistive-Ladder DAC
  - Use only two R and 2R resistor values, easy to manufacture.

Type 1: Weighted Adder DAC (E.g. N=8)

Resistor $=2^{(N-i)}*R$

i=8, $2^{8-8}R = R$

i=7, $2^{8-7}R = 2R$

:

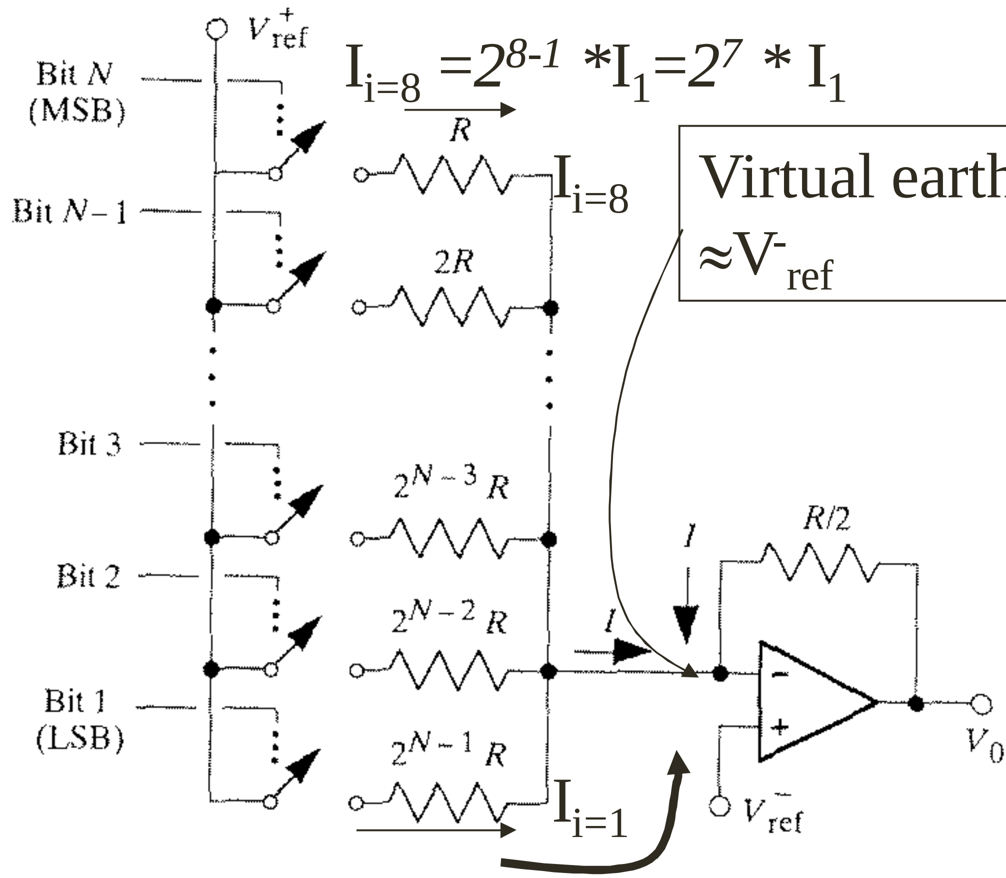
:

i=3, $2^{8-3}R = 2^5R$

i=2, $2^{8-2}R = 2^6R$

i=1, $2^{8-1}R = 2^7R$

$I_{i=8} = 2^{8-1} * I_1 = 2^7 * I_1$



Virtual earth $\approx V^-_{ref}$

$\Delta I = I_{i=1} = \text{Current} =$

$\Delta(V_{ref} - V_{-ref})/(2^{8-1}R) = (1/2^{8-1})[(V_{ref} - V_{-ref})/R]$

Resistor
R=2K
2R=4K
8K
16K
32K
64K
128K
128R=256K

Weighted Adder DAC (Cont'd)

- When ith bit (e.g. N=8, i=7 , N-i=1) = 1
  - ith analog switch (FET transistor) is turned on
  - I_i then flows thru. Resistor $2^{N-i}R$

$$\text{Where } I_i = \frac{V_{+ref} - V_{-ref}}{2^{N-i} R}:$$

$$\text{for bit 1(LSB), } \Delta I = \left[\frac{V_{+ref} - V_{-ref}}{2^{N-1} R} \right]$$

Weighted Adder DAC (Cont'd)

- When n has only one bit on

For an code n, which has only one bit on

$$I_n = n\Delta I = n\left[\frac{V_{+ref} - V_{-ref}}{2^{N-1}R}\right] = \frac{V_0 - V_{-ref}}{R/2}$$

input side

feedback side

rearrange terms and solving for V_0,

we have $V_0 = V_{-ref} + n\left[\frac{V_{+ref} - V_{-ref}}{2^N}\right]$

Weighted Adder DAC (Cont'd)

- When n has multiple on-bits
  - E.g. a 4-bit DAC, N=4. Input code=0101=n=n_3+n_1 (two bits are on)=binary{0100}+binary{0001}

$$V_{n3="0100"} = V_{-ref} + 4\left[\frac{V_{+ref} - V_{-ref}}{2^4}\right]$$

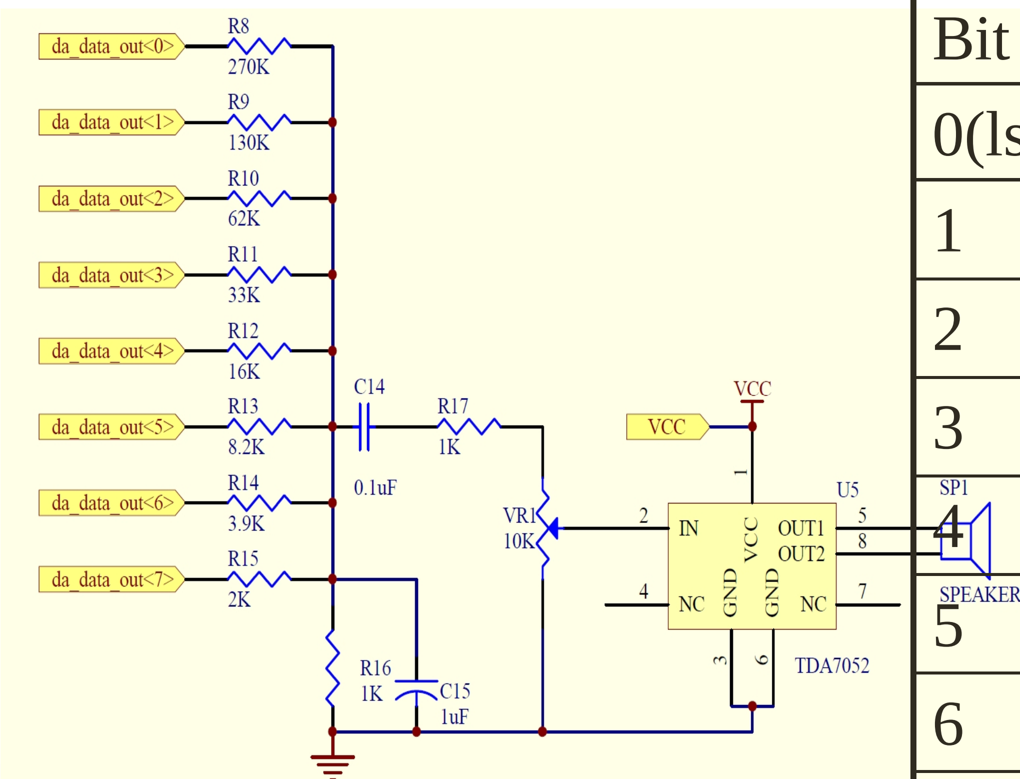
$$V_{n1="0001"} = V_{-ref} + 1\left[\frac{V_{+ref} - V_{-ref}}{2^4}\right]$$

$$V_{n=n1+n3="0101"} = V_{-ref} + 5\left[\frac{V_{+ref} - V_{-ref}}{2^4}\right]$$

** difficult to make because it uses a wide range of different Rs

Practical resistor network DAC and audio amplifier (not perfect but ok)

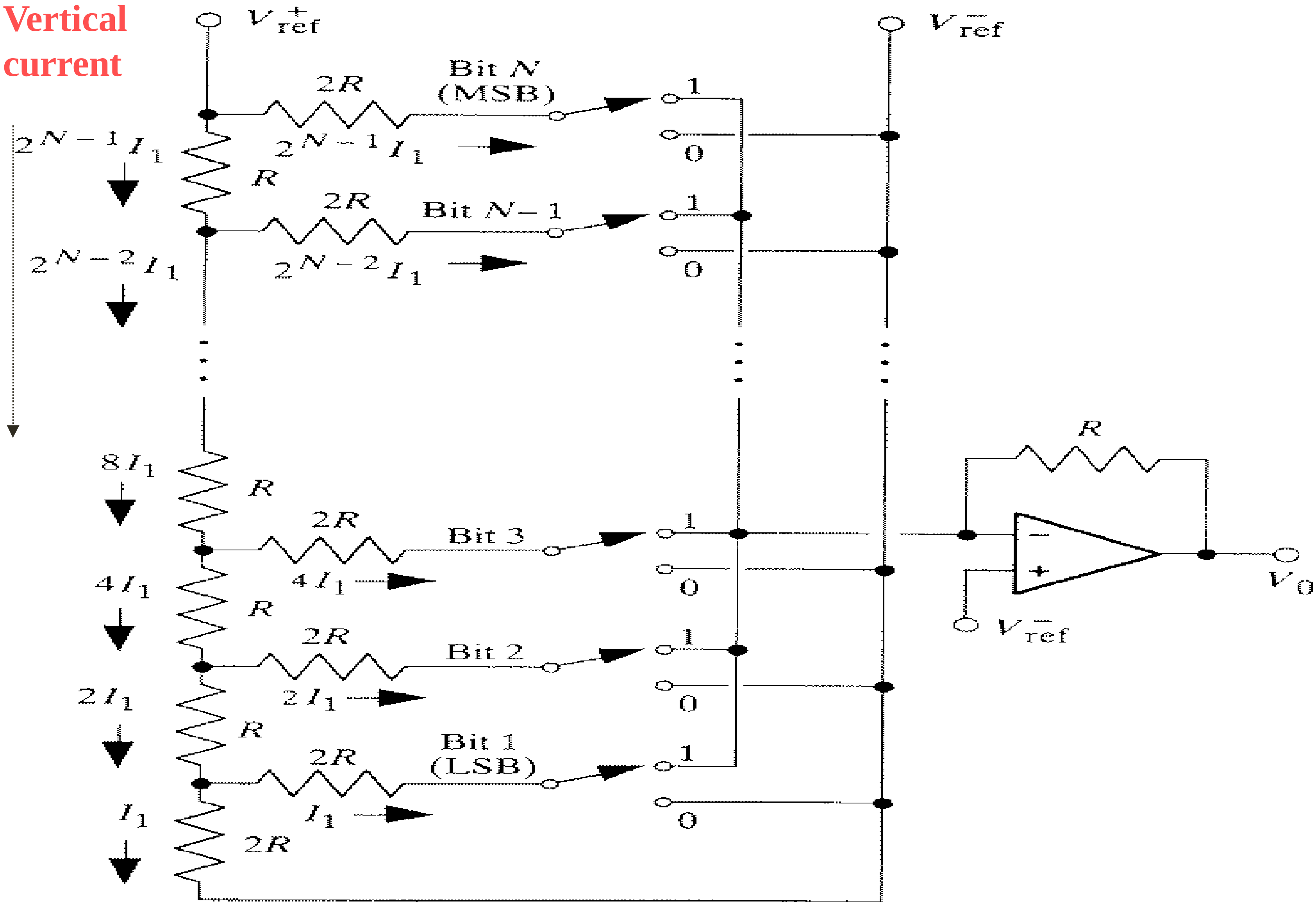
Set R=2K



Data Bit	i	Ideal R $=2^{8-i}R$	Practical
0(lsb)	1	256K	270K
1	2	128K	130K
2	3	64K	62K
3	4	32K	33K
4	5	16K	16K
5	6	8K	8.2K
6	7	4K	3.9K
7(msb)	8	2K	2K

Type 2: R-2R Resistive-Ladder DAC

Vertical current



DAC type2: R-2-R resistor-ladder

- Required only R & 2R, easy for IC fabrication process
- The most popular DAC
- At each node, current is split into 2 equal parts:
  - One goes to V-ref; the other goes to the op-amp negative-feedback point
- Where $$\Delta I_1 = \frac{V_{+ref} - V_{-ref}}{2^{N-1}(2R)} = \frac{V_{+ref} - V_{-ref}}{2^N R}$$
- Since inputs $V_+ \sim V_-$ of the opamp inputs are the same , the vertical current will not be changed by input code n

$$\frac{Vo - V_{-ref}}{R} = n\Delta I_1 = n\frac{V_{+ref} - V_{-ref}}{2^N R}, so$$

$$Vo = V_{-ref} + n\left(\frac{V_{+ref} - V_{-ref}}{2^N}\right)$$

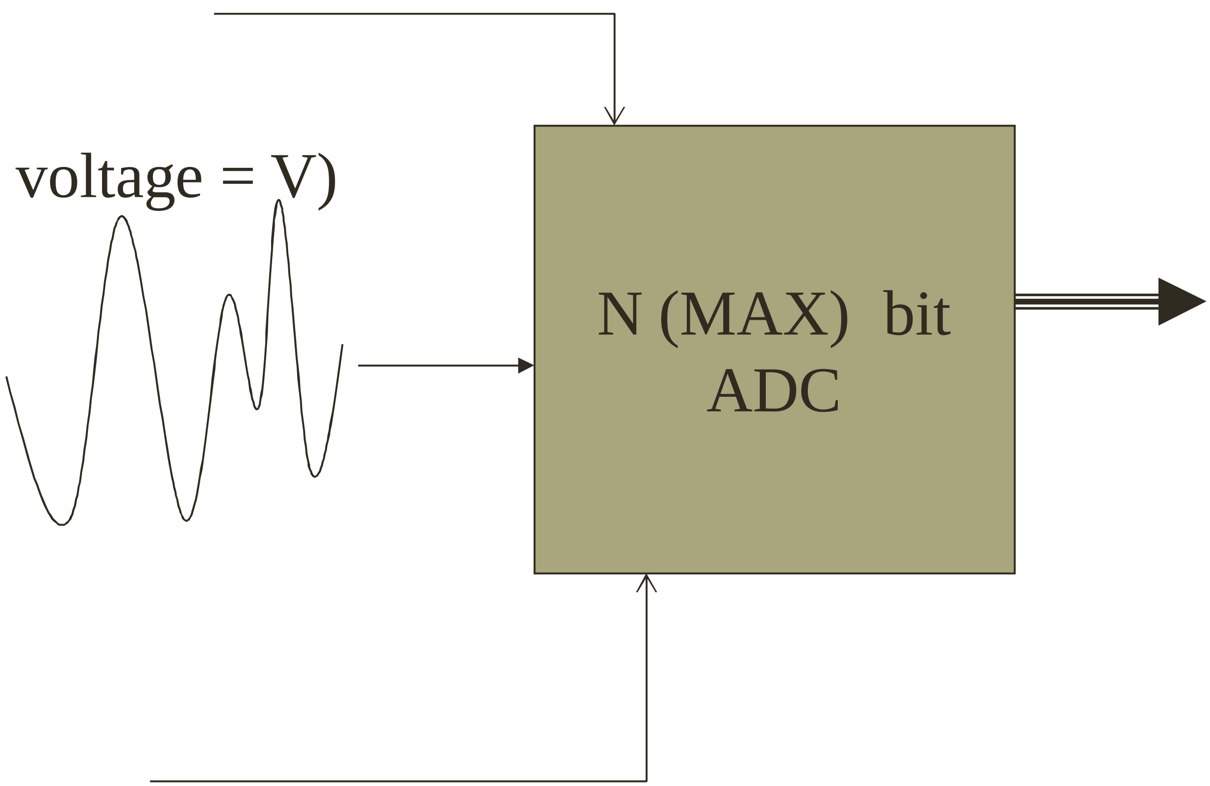
Analog to Digital Conversion

ADC

Analog to Digital Conversion ADC

- V_{+ref}

Input voltage = V)



V_{-ref}

output code = n
0110001
0100010
0100100
0101011
:
:
:

ADC Major characteristics

- *n*=converted code, *V*=input voltage,

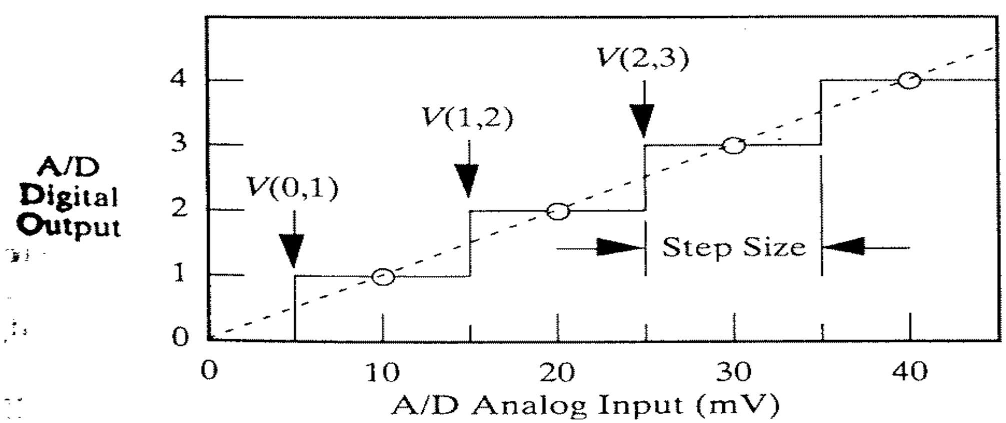
$$n = \left[\frac{V - V_{-ref}}{\Delta V} + \frac{1}{2} \right]_{\text{integer}}, \text{where } \Delta V = \frac{V_{+ref} - V_{-ref}}{2^N - 1},$$

$$e.g\ V_{-ref} = 0,\ \Delta V = 10mV, \text{ see the figure on next page.}$$

- The linearity measures how well the transition voltages lie on a straight line.
- The differential linearity measures the equality of the step size.
- Conversion time:between start convert and result generated
- Conversion rate=inverse of conversion time

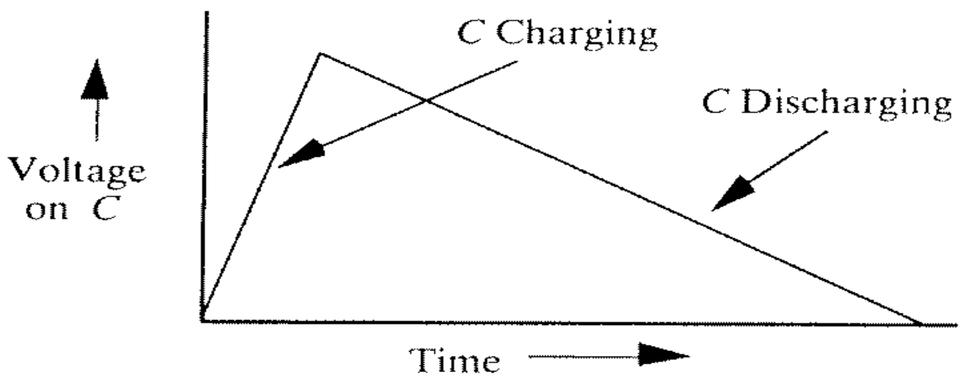
Analog to digital converter example

- Convert an analog level to digital output
- From [1], e.g. V_{-ref}=0V, ΔV=10mV.



ADC Type 1: Integrating or dual slope

- Accumulate the input current on a capacitor for a fixed time and then measure the time (T) to discharge the capacitor at a fixed discharge rate.
  - 1) S_1->V_1:Integrate the input on the cap. For N clock ticks
  - 2) S_1-> -Vref: restart clock (S2->counter) discharge C at know rate(governed by -Vref and R)
  - 3) When the cap. is discharged to 0 voltage, the comparator will stop the counter.

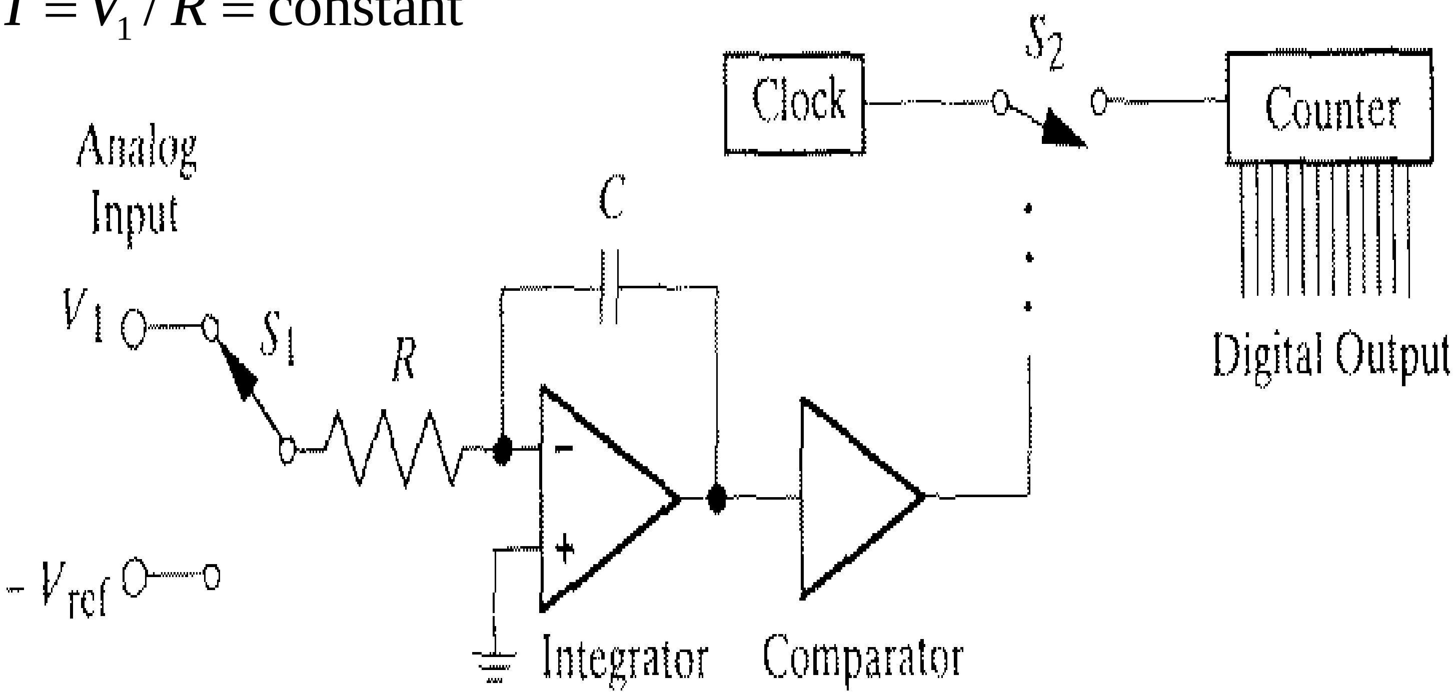


problem --very slow

Integrating dual slope ADC: Simplified Diagram

$$charge\_held = Q = \int_0^{T = fixed} I dt$$

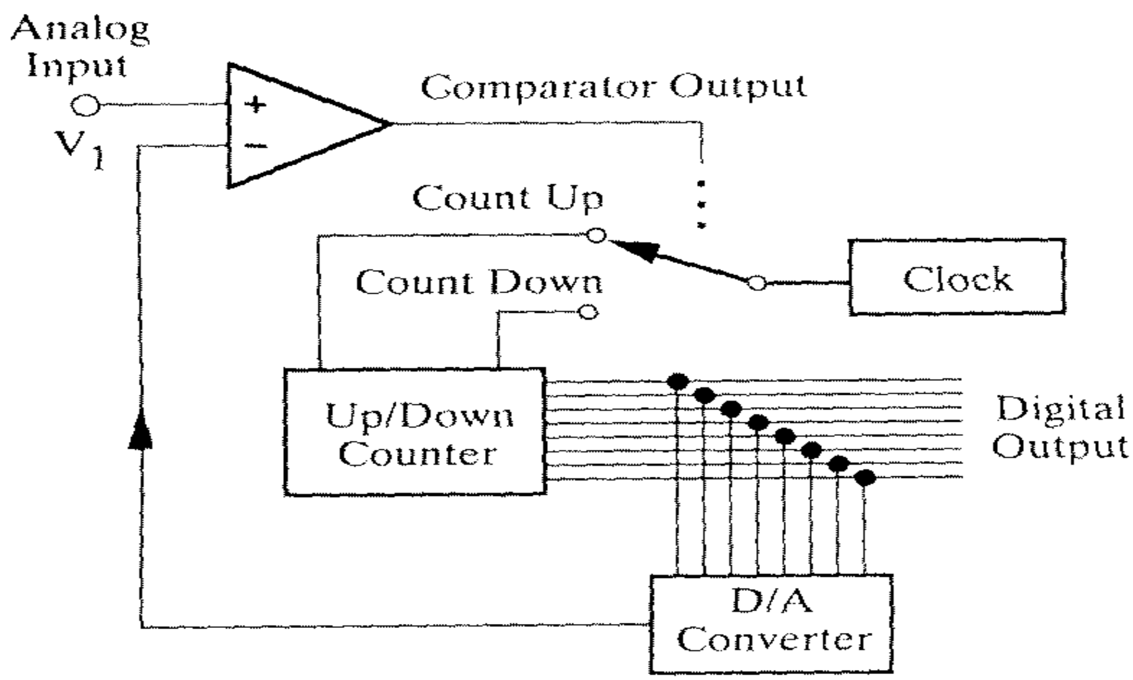
- $I = V_1 / R = \text{constant}$



Discharge time for stopping counter by S_2 depends on RC and Q

Type 2: Tracking ADC

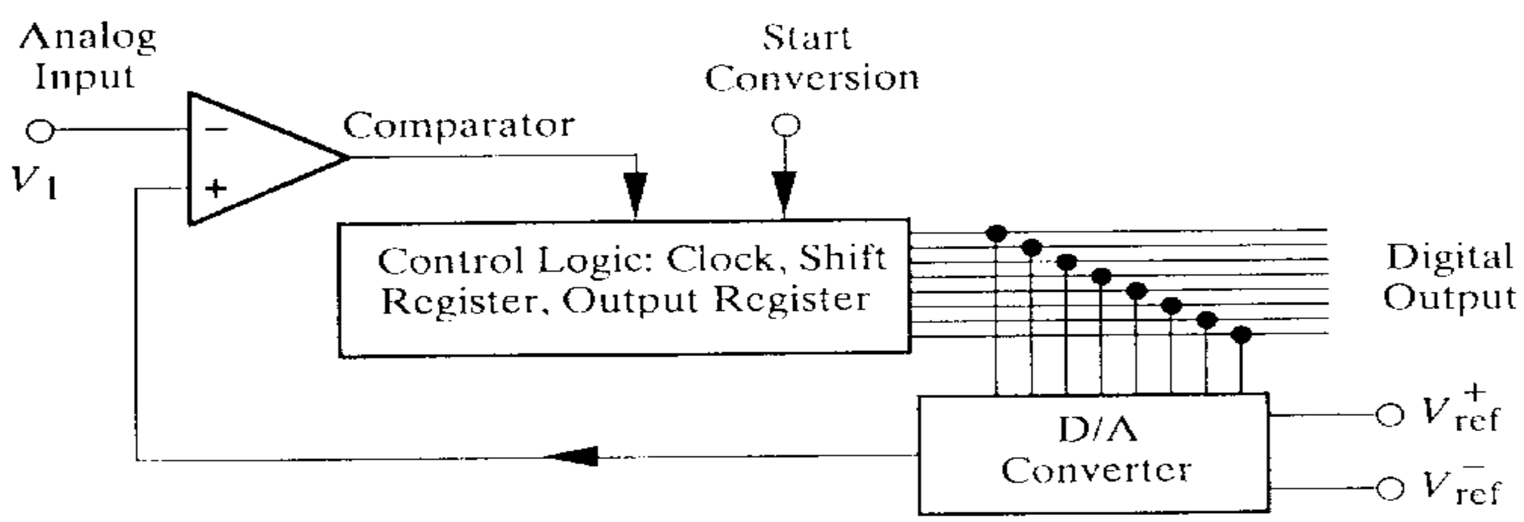
- The ADC repeatedly compares its input with DAC outputs.
- Up/down count depends on input/DAC output comparison.



problem –also slow

Type 3 ADC : successive approximation

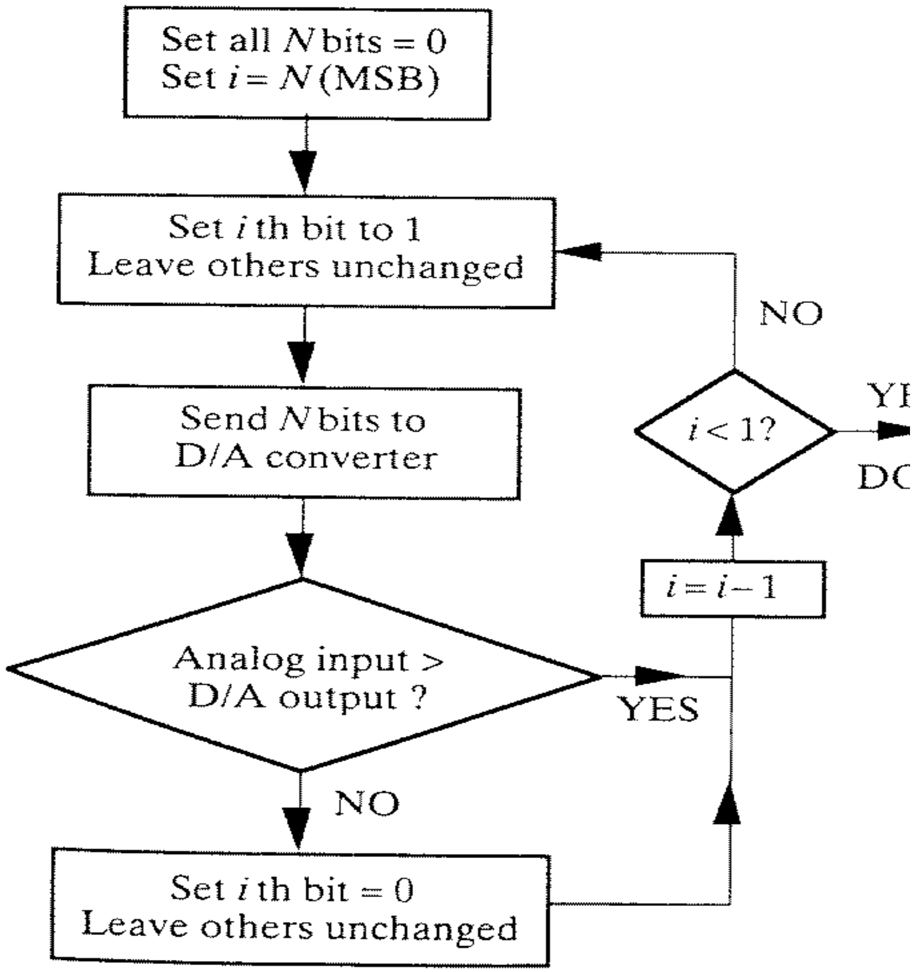
- Faster, use binary search to determine the output bits.



problem –still slow although faster than types 1 & 2

Flow chart of Successive-approximation ADC

•

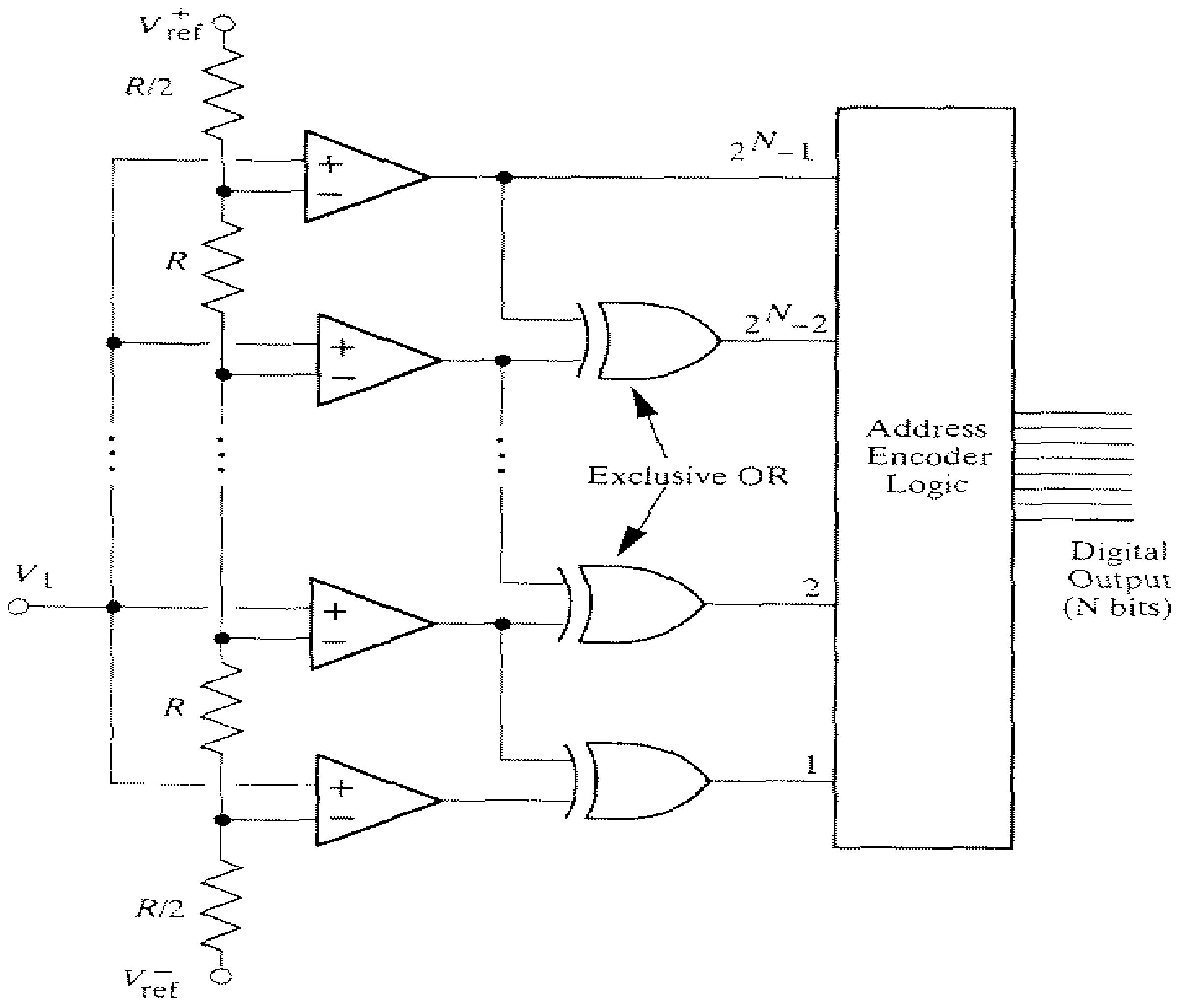


Yes, done

Type 4 ADC : Flash ADC (very fast)

- Divide the voltage range into 2^N-1 levels; use 2^N-1 comparators to determine what the voltage level is
- Use a 2^N-1 input to N bit priority decoder to work out the binary number

Diagram of a flash ADC [1]



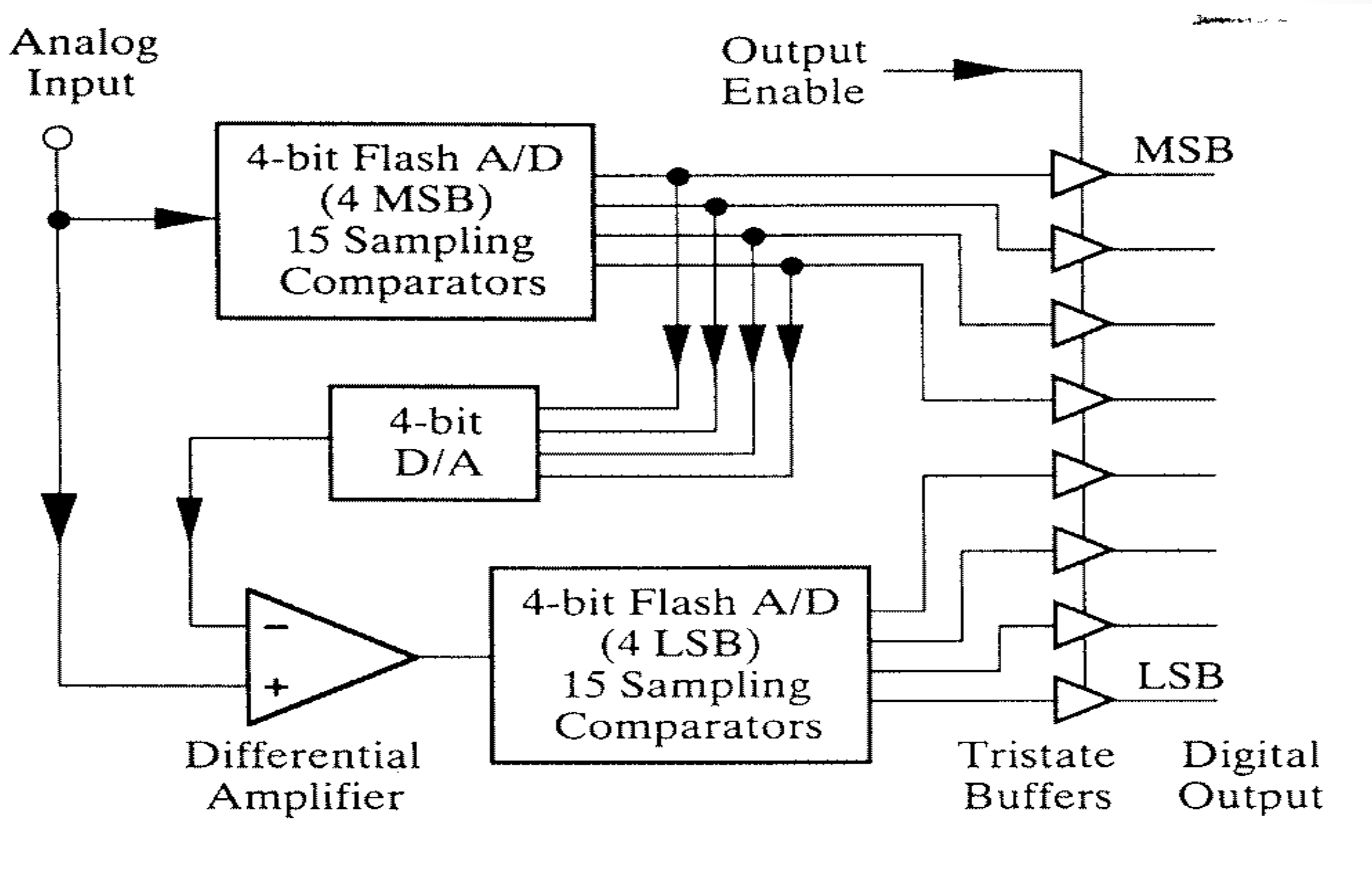
Type 4 ADC : Flash ADC (cont'd)

- Very fast for high quality audio and video.
- Very expensive for wide bits conversion.
- Sample and hold circuit usually **NOT** required.
- The number of comparators needed is 2^N-1 which grows rapidly with the number of bits
  - E.g. for 4-bit, 15 comparators;
  - for 6-bit, 63 comparators.

Type 5 ADC : subranging Flash ADC

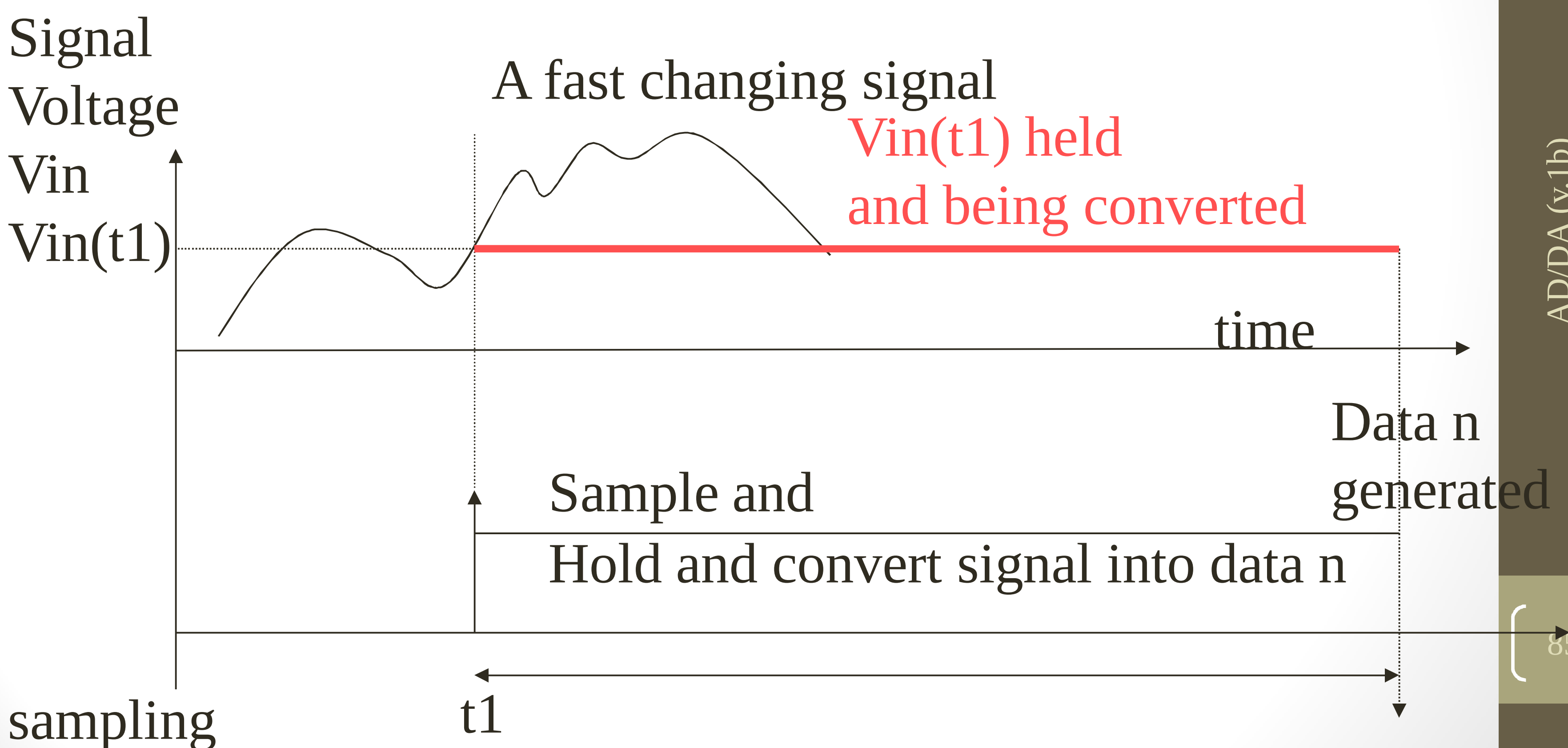
- Compromise; medium speed
- Pure Flash ADC is very expensive for large number of bits.
- Subranging Flash ADC is Hybrid between successive approximation and flash.
- AD7280 or ADC0820 uses two 4-bit flash ADC to build an 8-bit subranging Flash ADC.
- Figure next page: Upper 4-bit (MSB) flash ADC finds coarse MSB digital output, then converts into approximate analog level by a 4-bit DAC, the lower 4-bit flash ADC finds the fine 4-bit (LSB) digital code.

Diagram of a subranging Flash built from two 4-bit flash ADC, [1]

- 

Sampling and hold?

Why? It is because when a slow ADC is used to sample a fast changing signal only a short sampling point can be analyzed



Sampling-speed limitation

- Given the conversion time of an ADC is T_{conv} seconds, the maximum sampling rate is F_{max}=1/T (Hz) .
  - E.g: ADC0801,
  - T_{conv} =114ns+μP to ADC delay,
  - F_{max}< 8.77KHz
- For this sample rate the maximum frequency for the input is (F_{max}/2) < 4.39KHz by Nyquist sampling theory.
- Need to use a sample-and-hold circuit to freeze a fast changing input when using a low speed ADC to convert the signal.
- For high speed conversion, use Direct-Memory-Access (DMA) to copy the data directly to μP memory to reduce μP to ADC delay.

Frequency aliasing

- When the highest frequency of the signal F_{input} is greater than half the sampling ($F_{sampling}/2$).
  - E.g. F_{input} =20KHz,
  - $F_{sampling}$ must be over 40KHz.
- Remedy: Use a low pass filter to cut off the input high frequency content before ADC sampling.

upper => sampling 6 times per cycle(fs=6f);
middle => sampling 3 times per cycle(fs=3f);

lower=> sampling 6 times in 5 cycles, from[1]

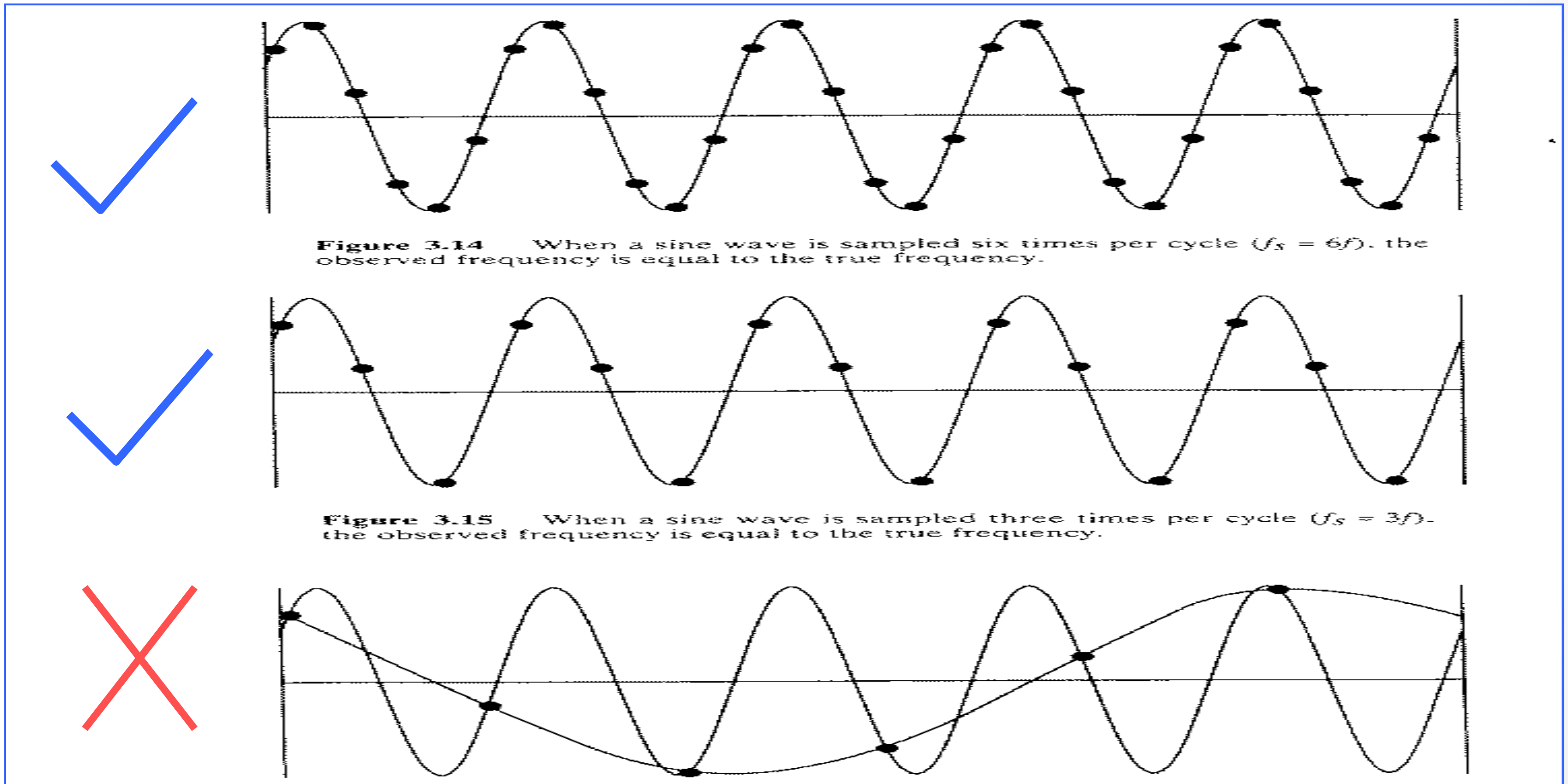
- 

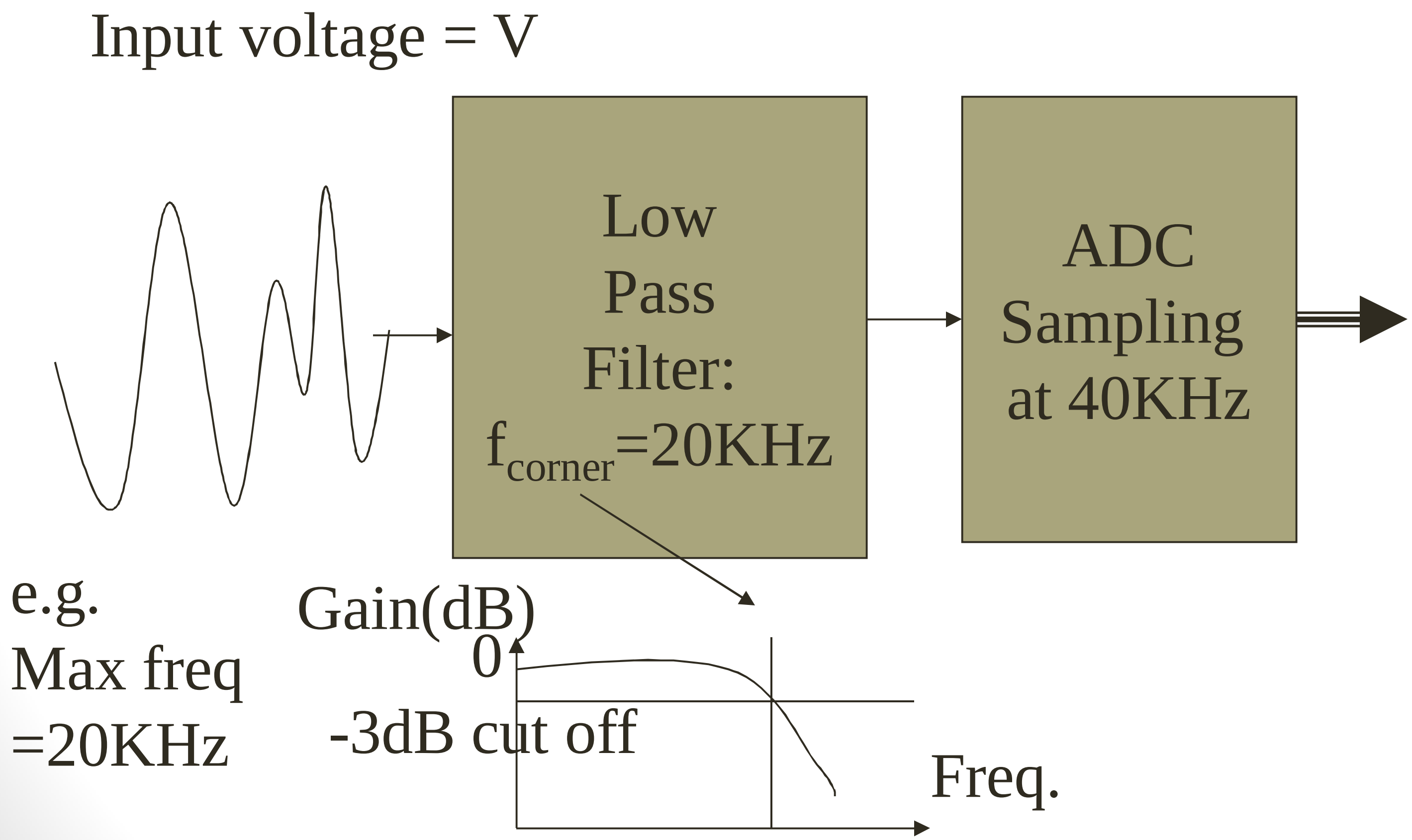
Figure 3.14 When a sine wave is sampled six times per cycle ($f_s = 6f$), the observed frequency is equal to the true frequency.

Figure 3.15 When a sine wave is sampled three times per cycle ($f_s = 3f$), the observed frequency is equal to the true frequency.

Figure 3.16 When a sine wave is sampled six times in five cycles, the observed sine wave has a much lower frequency than the original sine wave.

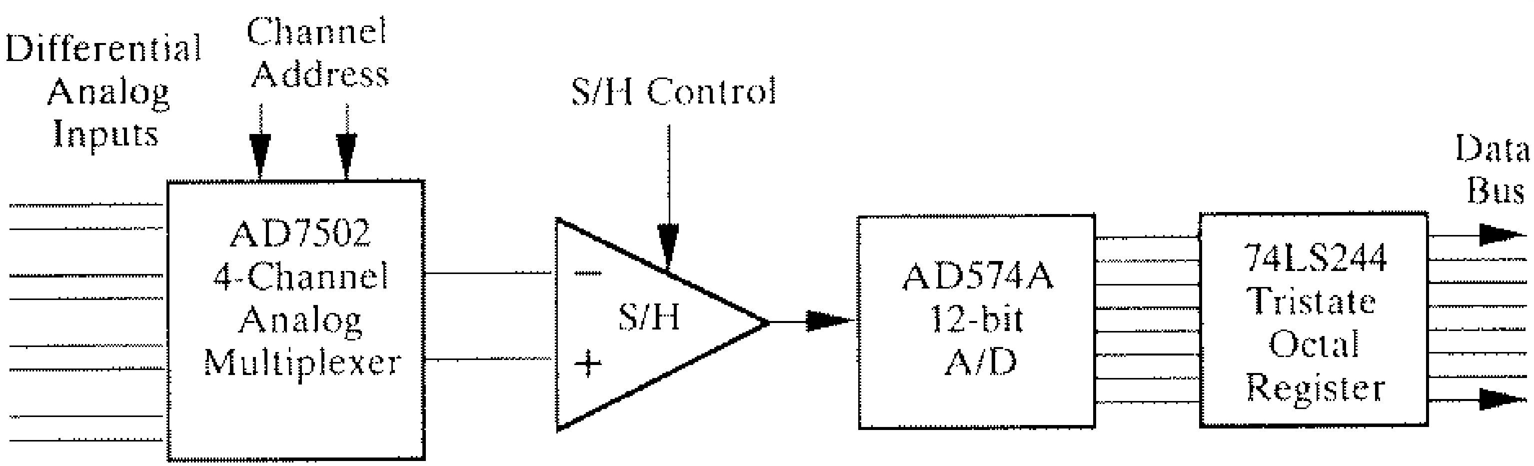
Method to reduce aliasing noise

- Use low pass filter to remove high frequenc before sampling



output code = n
0110001
0100010
0100100
0101011
:
:
:

Commercially available multiple input channels ADC board with channel select and sample-and-hold



Practical ADCs

- Low cost, low speed (successive approximation, 8bit-8KHz sampling), National semiconductor ADC0801,2,3,4 family. See http://www.national.com/catalog/
- Medium speed (half-flash, 8-bit 666KHz), National semiconductor ADC0820.
- High speed (flash 8-bit,40~80MHz, video quality) Philips TDA8714 (/7/6/4) family. See http://207.87.19.21/products/

ADC0801 description from http://www.national.com/catalog/

- 8-bit successive approximation A/D converters that use a differential potentiometric ladder-similar to the 256R products.
- Output latches directly driving the data bus.
- These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.
- Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value.
- Voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

ADC0801 features

- Compatible with 8080 µP derivatives-no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone" .
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3[Foot][Minute][Prime] standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 VDC, 2.5 VDC, or analog span adjusted voltage reference

ADC0820 half-flash ADC, from http://www.national.com/catalog/

- The half-flash 8-bit ADC0820 A/D offers a 1.5 µs conversion time
- The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a L.S. 4-bit ADC.
- The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/µs.
- For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

ADC0820 features

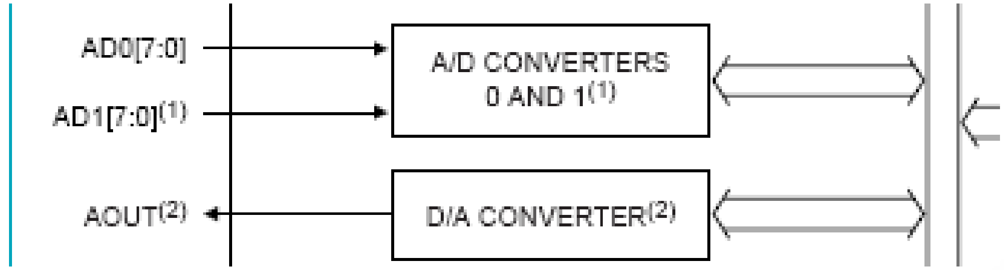
- Built-in track-and-hold function
- No missing codes , no external clocking
- Single supply-5 VDC. Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than VCC
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading

ARM7(MCU)– LPC2131/32 has built-in ADC & DAC

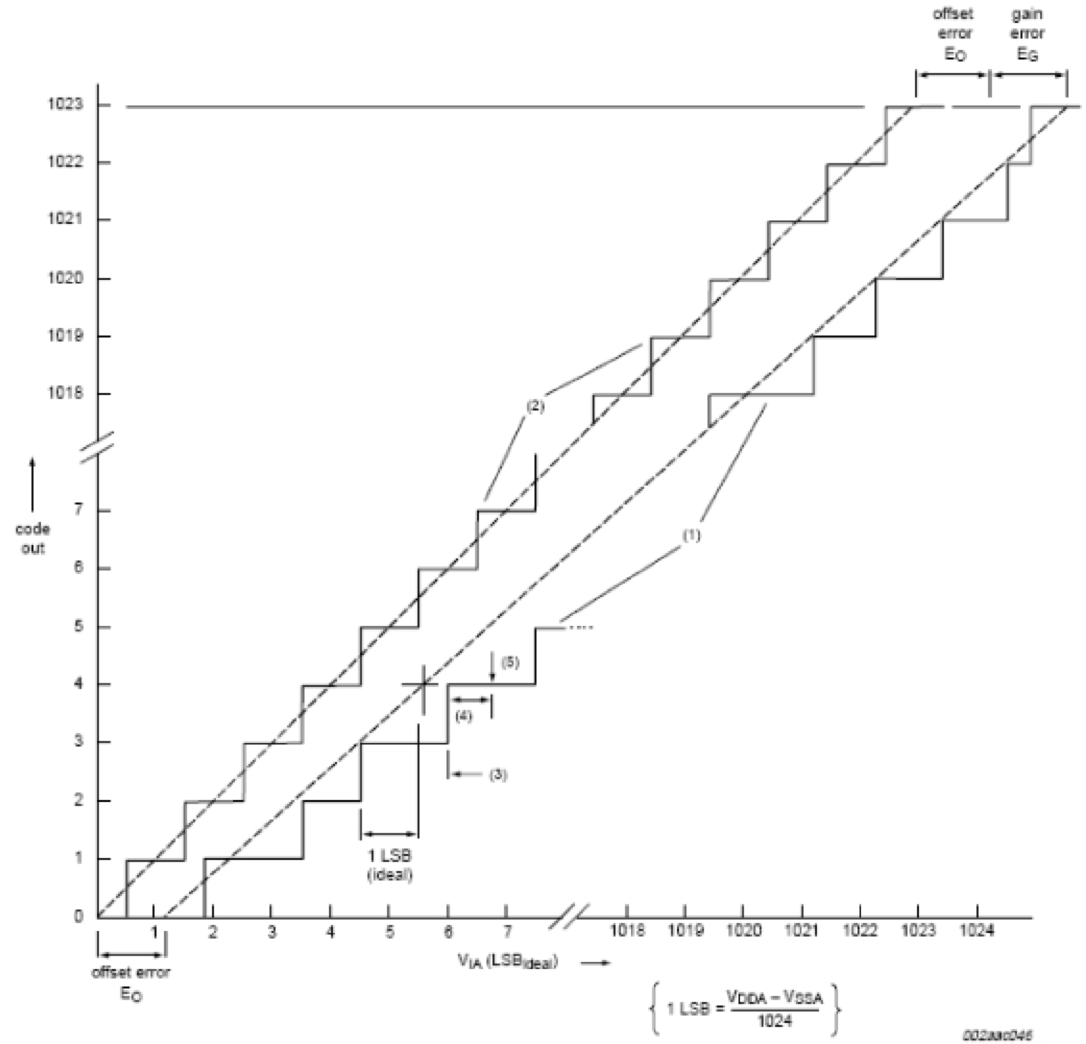
www.hitex.co.uk

http://www.nxp.com/pip/LPC2132FBD64.html

- *One (LPC2131/32) or two (LPC2134/36/38) 8-channel 10-bit ADCs provide a total of up to 16 analog inputs, with conversion times as low as 2.44 us per channel.* (sampling freq<1/2.44us=0.9MHz=900KHz)??
- A single 10-bit DAC provides variable analog output (LPC2132/34/36/38).



ADC characteristic



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 7. ADC characteristics

Assignment

- Explain A/D and D/A converters

Waveforms

Frequency and Time Measurement & Conversion

Asynchronous Counter

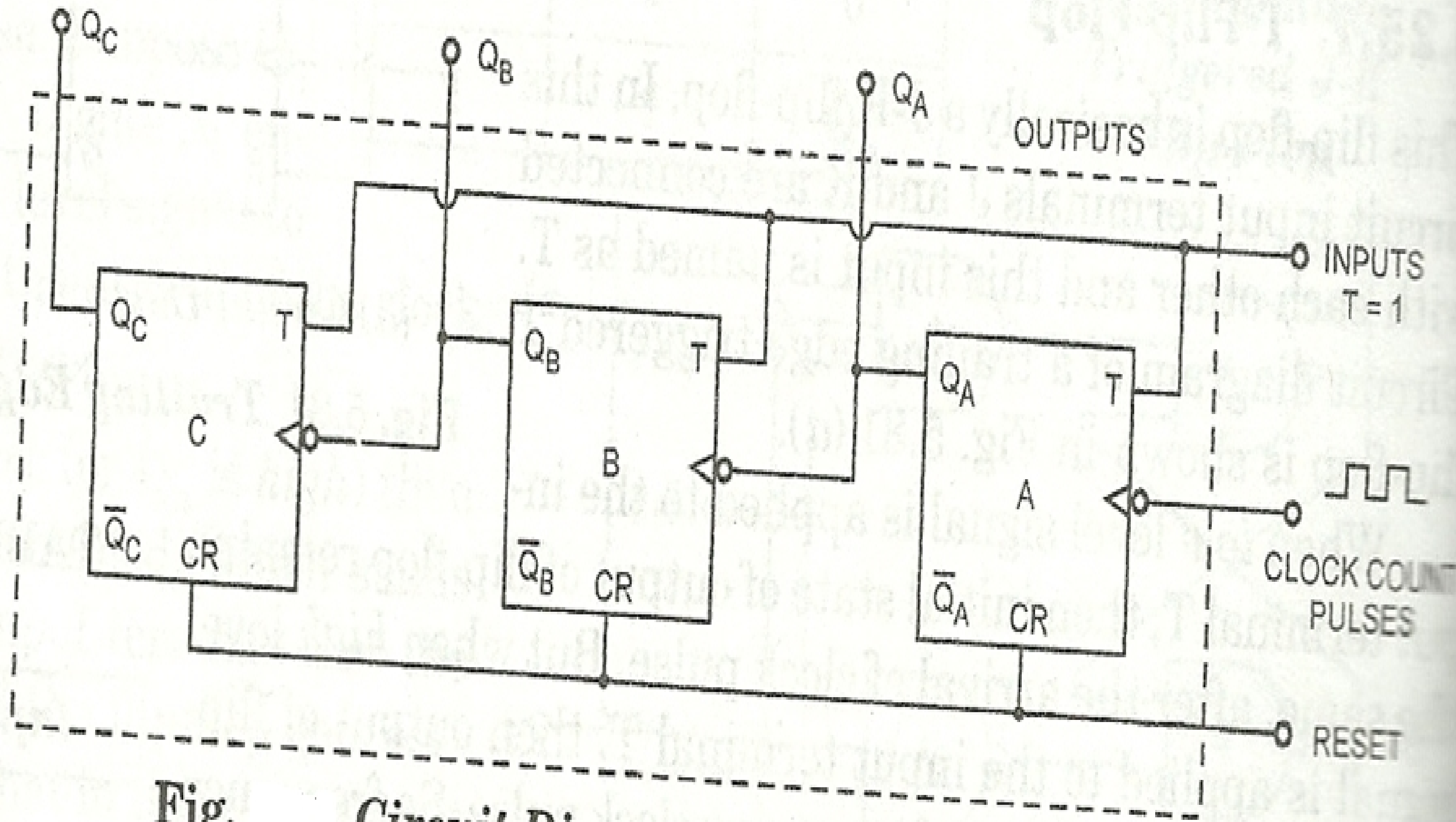


Fig. ***Circuit Diagram of a 3-bit Ripple Counter***

Asynchronous Counter

Q_C	Q_B	Q_A	Clock Count Pulse
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8 (recycles)

Synchronous Counter

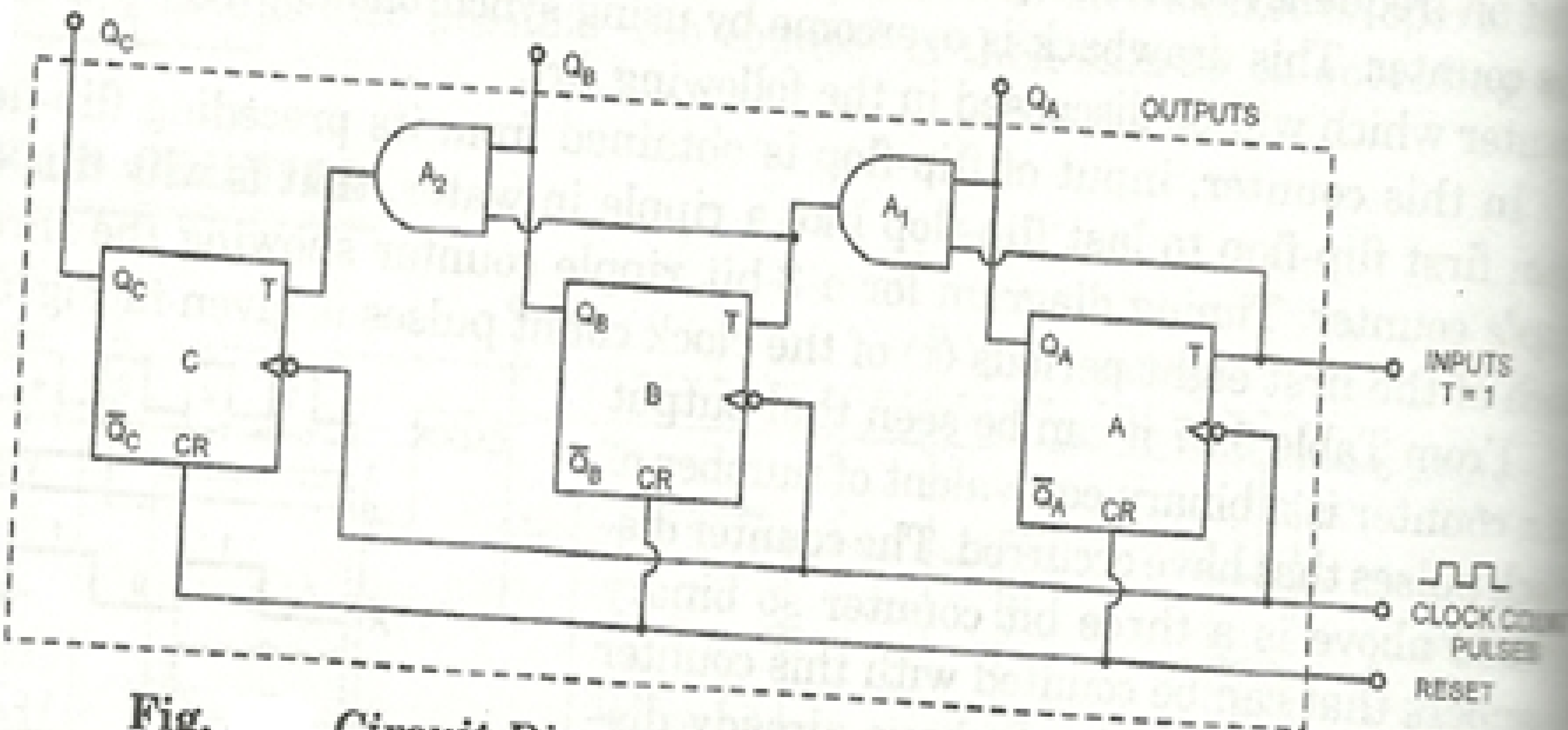


Fig. ***Circuit Diagram of a 3-bit Synchronous Counter***

Ring Counter

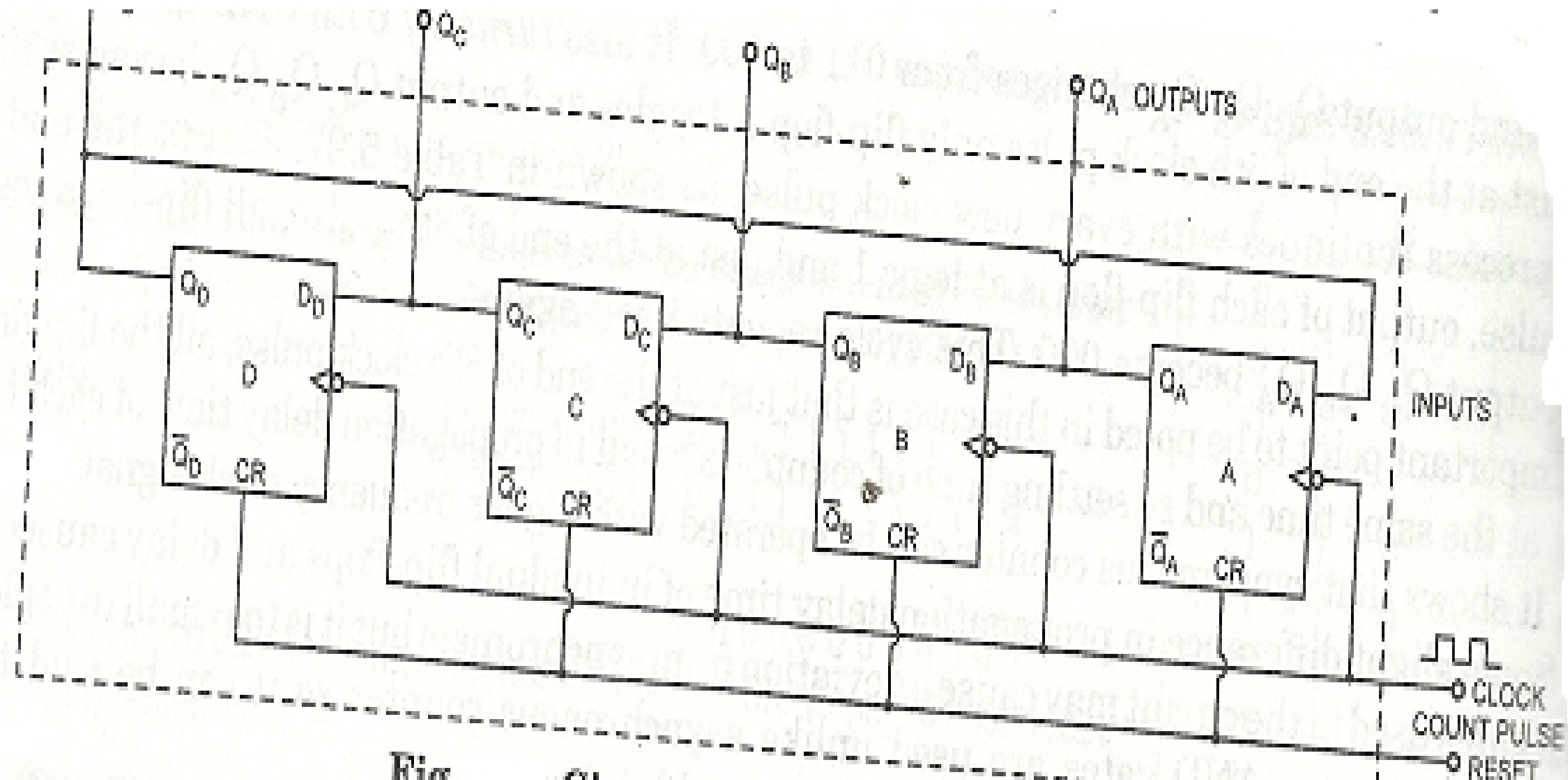


Fig. ***Circuit Diagram of Ring Counter***

Decimal or Decade Counter

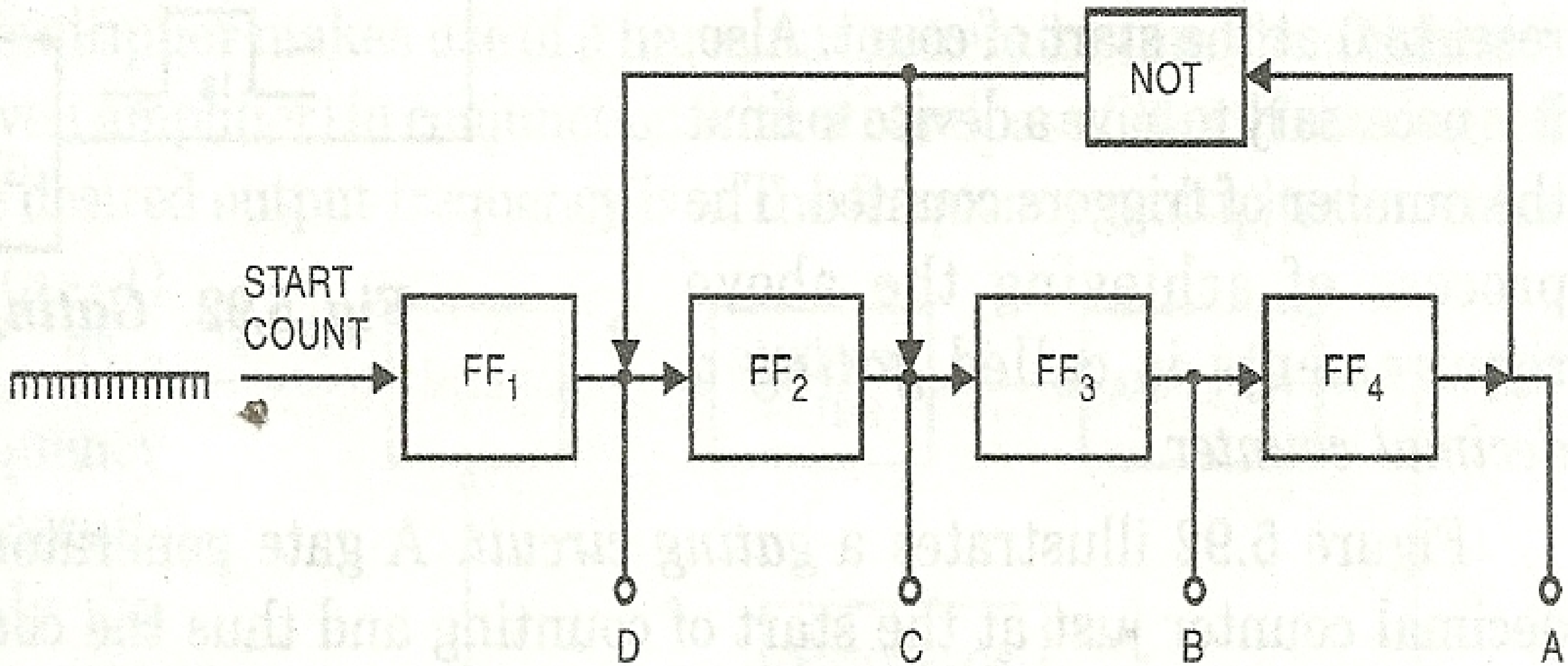


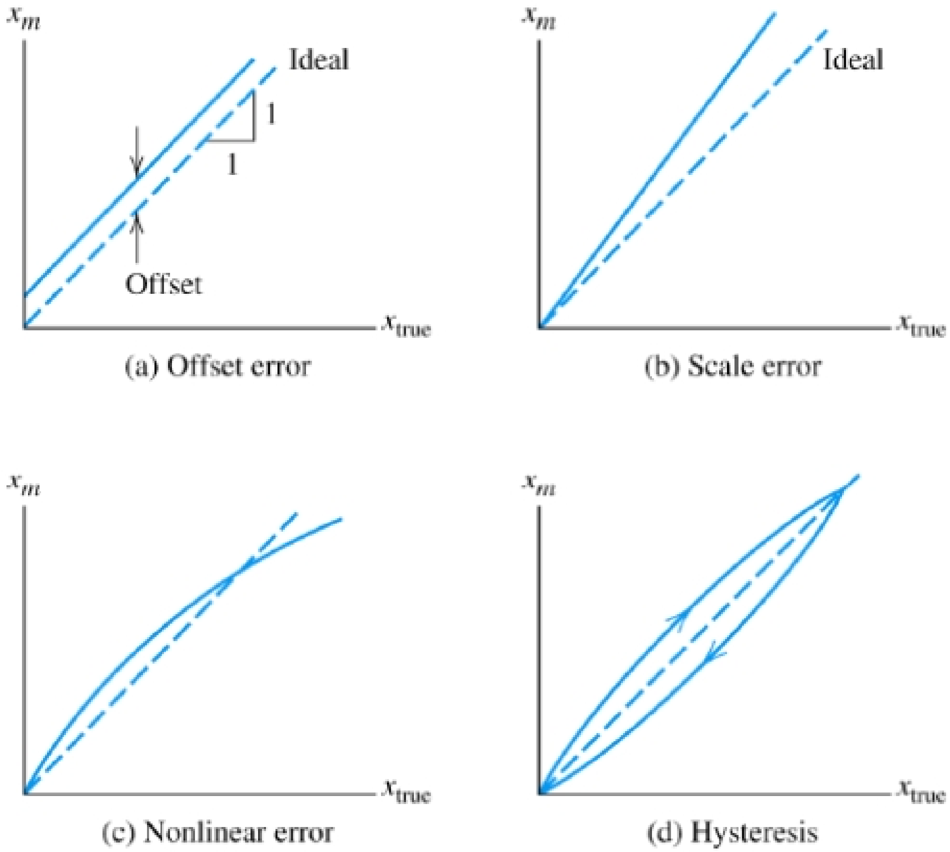
Fig. ***Block Diagram of a Decimal Counter***

Decimal or Decade Counter

TABLE Truth Table for Decade Counter

Number of Triggers	*A*	*B*	*C*	*D*
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	1	0
9	1	1	1	1
10	0	0	0	0

Typical errors



Statistics

- Value distribution:
  - Average deviation (data dispersion):

$$\sigma = \frac{\sum |d_i|}{n}$$

  - Standard deviation:
    - n->(n-1) if n<20

$$s = \sqrt{\frac{\sum d_i^2}{n}}$$

  - Correlation of data:
    - Linear regression:

$$Y = mX + b$$

$$m = \frac{n\sum(XY) - \sum X \sum Y}{n\sum(X^2) - \left(\sum X\right)^2}$$

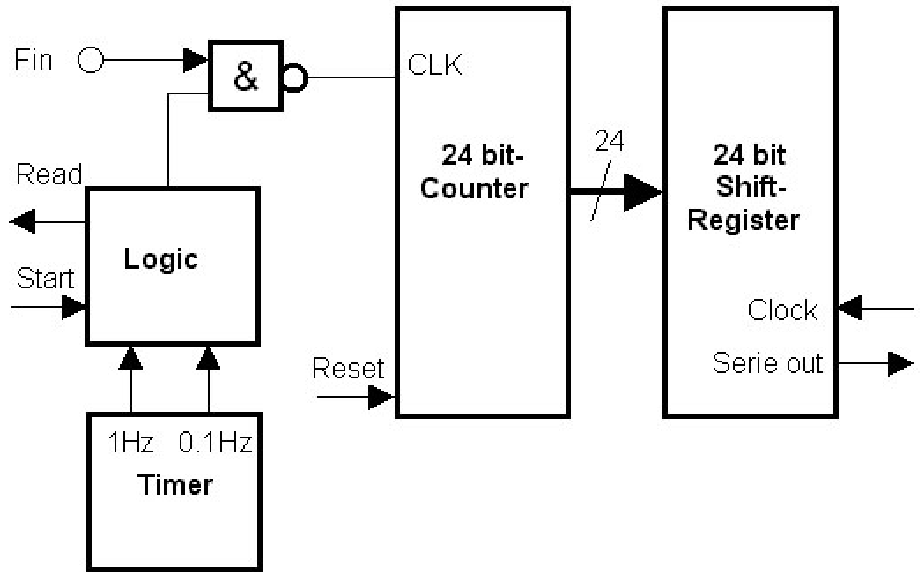
$$b = \frac{\sum Y(\sum X^2) - \sum X \sum(XY)}{n\sum(X^2) - (\sum X)^2} = \frac{\sum Y - m\sum X}{n}$$

Signal generators
Arbitrary waveforms

- Oscillators (sinusoidal waveforms)
- Signal generators (RF)
- Function generators
- Arbitrary waveforms generators
  - Analog
  - Digital (DAC based)
- Synthesizers (base frequencies)

Frequency counters

- Frequency
- Period
- Event counter
- Frequency rates
- Time intervals



Modulators and Demodulators

Amplitude and Phase Modulation and Demodulation

- Amplitude modulation (AM) is the process of varying the amplitude of a constant frequency signal with a modulating signal. An amplitude-modulated wave can be mathematically expressed as $S(t) = g(t)\sin\omega_c t$ where *g(t)* is the modulating signal and ω_c is the carrier frequency. Normally the modulating signal varies slowly compared with the carrier signal frequency. Conventional AM is in the form of $S(t) = A[1 + mf(t)]\sin\omega_c t$ where *m* is the modulation factor and is normally less than 1. Consider a simple modulating signal:

$$f(t) = \cos\omega_m t \quad \text{then} \quad S(t) = A\left\{\sin\omega_c t + \frac{m}{2}[\sin(\omega_c + \omega_m)t + \sin(\omega_c - \omega_m)t\right\}$$

- The frequency spectrum of the modulated signal is shown

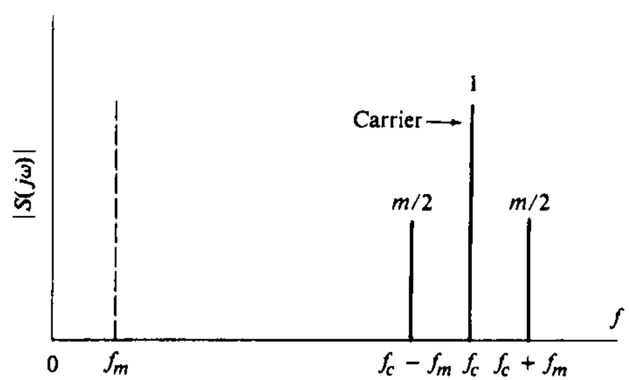


FIGURE 12.25
Frequency spectrum of an amplitude-modulated signal.

- The equation above shows that for m<1 the amplitude of the carrier is at least twice as large as the amplitude of either sideband component, so at least 2/3 of the signal power will be in the carrier and at most 1/3 in the 2 sidebands. Because the carrier does not contain any information, it is often removed or suppressed in the signal

$$S(t) = \frac{Am}{2}[\sin(\omega_c + \omega_m)t + \sin(\omega_c - \omega_m)t]$$

which is referred to as a double-sideband (DSB) suppressed-carrier signal. The carrier component is not present in the DSB signal. However, as the waveform gets more efficient in terms of power-to-information content, the detection method gets more complex. Some means of recovering the carrier component is needed for the detector to recover the amplitude and frequency of the modulating signal. The DSB signal, although more efficient in terms of transmitted power, still occupies the same bandwidth as a normal AM signal. Since both sidebands contain the same information, one sideband can be removed, resulting in a *single-sideband-signal* (SSB).

Amplitude Modulators

- Full-carrier double-sideband amplitude modulation is achieved either modulating the oscillator signal at a relatively low power level and amplifying the modulated signal with a cascade of amplifiers or by using the modulating signal to control the supply voltage o fthe power amplifier. Both methods are illustrated below

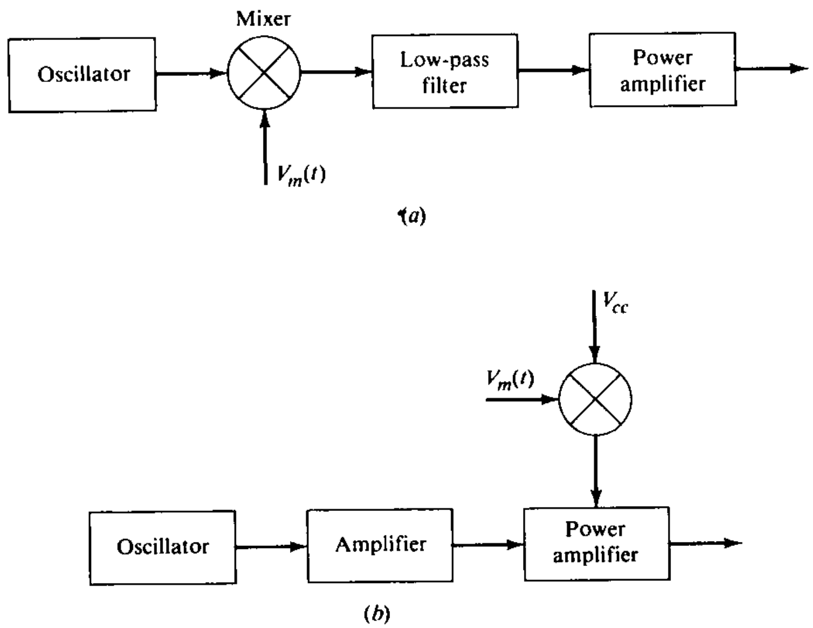


FIGURE 12.27
(*a*) A low-level amplitude-modulation circuit; (*b*) amplitude modulation at high power levels.

the amplifier output circuit is not current-limited.

- The most frequently used method of amplitude modulation at high power levels is to modulate the supply voltage to the power amplifier, as shown in Fig. 12-27b. In the figure below

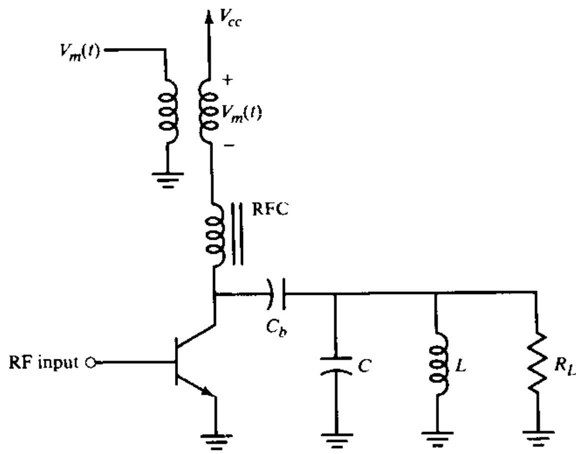


FIGURE 12.28
A collector-modulated circuit.

the modulating signal is applied in series with the dc supply voltage, so the total low-frequency supply for the transistor is

$$V = V_{CC} + V_m(t); \qquad = V_{CC}(1 + m\cos\omega_m t)$$

$$V_m(t) = mV_{CC}\cos\omega_m t$$

sidebands with a filter. A block diagram of this form of SSB is shown below

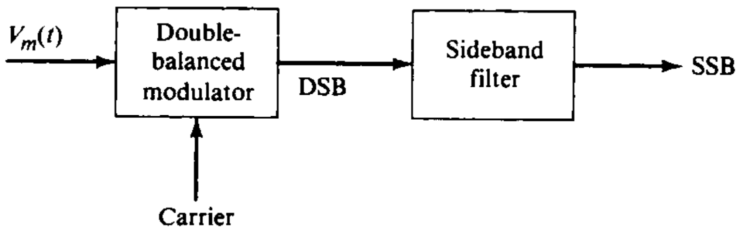


FIGURE 12.29
Filtering method of single-sideband generation.

- Another technique know as phasing method is shown below:

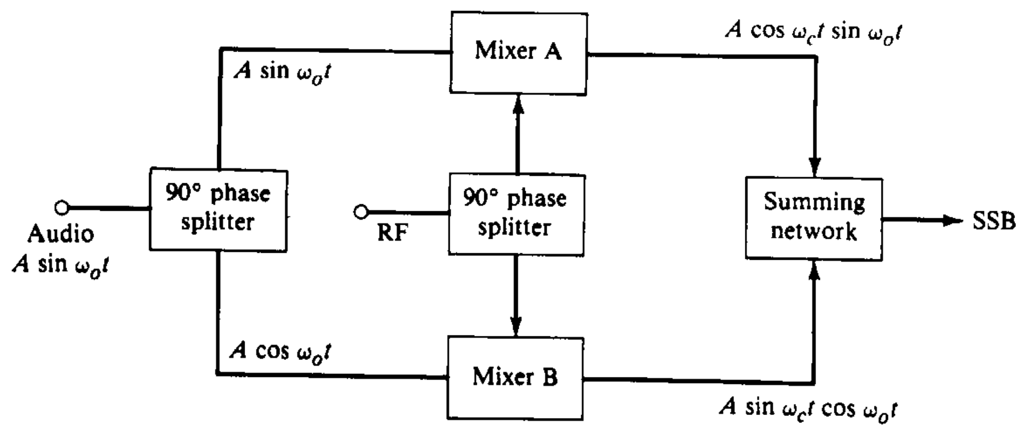


FIGURE 12.30
Phasing method of single-sideband generation.

- Here both the modulating signal and the carrier signal are processed through phase splitters, which each generate two signals 90° out of phase with each other. The summing network output

$$S(t) = A\cos\omega_c t \sin\omega_o t + A\sin\omega_c t \cos\omega_o t$$

$$= A\sin(\omega_c + \omega_o)t$$

is the desired SSBsignal. The phasing method has the advantage of not requiring the sharp cutoff filters of the filtering method of SSBgeneration, but it is difficult to realize a broadband phase-shifting network for the lower frequency modulating signal.

Demodulators

- AM detection can be divided into synchronous and asynchronous detection. Synchronous detection employs a time-varying or nonlinear element synchronized with the incoming carrier frequency. Otherwise the detection is asynchronous. The simplest asynchronous detector, the average envelope detector, is described below:

Average Envelope Detectors

- A block diagram of the average envelope detector is shown in the fig.

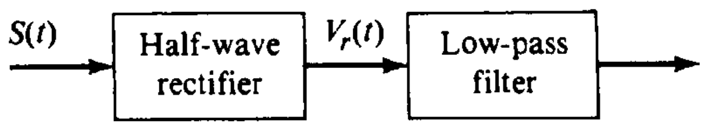


FIGURE 12.31
Block diagram of an average envelope detector.

- The rectifier output $V_r(t) = \begin{cases} S(t) & S(t) > 0 \\ 0 & S(t) < 0 \end{cases}$
- can be written as $V_r(t) = S(t)P(t)$
- If S(t) is periodic with a frequency ω_c, since $P(t) = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{\infty} \frac{\sin(2n+1)}{2n+1}\omega_c t$
- If S(t) is the AM wave described by $S(t) = A[1 + mf(t)]\sin\omega_c t$

$$V_r(t) = A[1 + mf(t)]\left(\frac{\sin\omega_c t}{2} + \pi^{-1} + \frac{\cos 2\omega_c t}{\pi} + \text{higher harmonics of } \omega_c\right)$$

- If the low-pass filter bandwidth is chosen to filter out the component at ω_c and all higher harmonics, the output will be $V_o(t) = \frac{A[1+mf(t)]}{\pi}$ which is a dc term plus the modulating information.
- Two additional points will be made to further describe the operation of the envelope detector. First, consider the case where $f(t) = \sin\omega_m t$
- The

$$V_r(t) = A\left[\frac{\sin\omega_c t}{2} + \frac{m}{\pi}\sin\omega_m t + \pi^{-1} + \pi^{-1}\frac{\cos(\omega_c - \omega_m)t - \cos(\omega_c + \omega_m)t}{2} + \text{higher frequency terms}\right]$$

- The output will contain a term at the frequency $\omega_c - \omega_m$, which must also be removed by the low-pass filter. This is not possible if ω_m is close to ω_c. To ensure this distortion does not occur the max modulating frequency should be $(\omega_m)_{\max} \le \frac{\omega_c}{2}$ and the corresponding low-pass filter bandwidth B must be selected so that $V_r(t) > 0$ if $S(t) > 0$
- This is only possible if *m* is not greater than 1, and the carrier term is present. Average envelope detection will only work for normal AM with a modulation index less than 1. However, if a large carrier component $A\cos\omega_c t$ is added to the SSB signal, the resultant signal can also be detected with an envelope detector.

- A simple diode envelope detector circuit is shown in the figure below

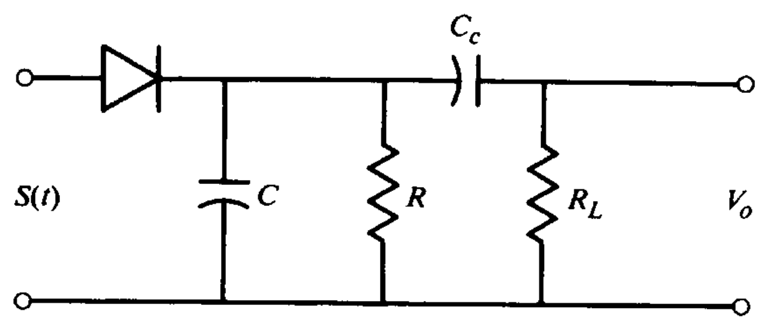


FIGURE 12.32
A diode envelope detector.

- It is assumed here that the input signal amplitude is large enough that the diode can be considered either on or off, depending upon the input signal polarity. The diode can then be replaced by a open circuit when it is reverse-biased and by a constant resistance when it is forward-biased. The series capacitor C_c is included to remove the dc component. The purpose of the load capacitor C in the circuit is to eliminate the high-frequency component from the output and to increase the average value of the output voltage. The effect of the load capacitor can be seen from the figure below

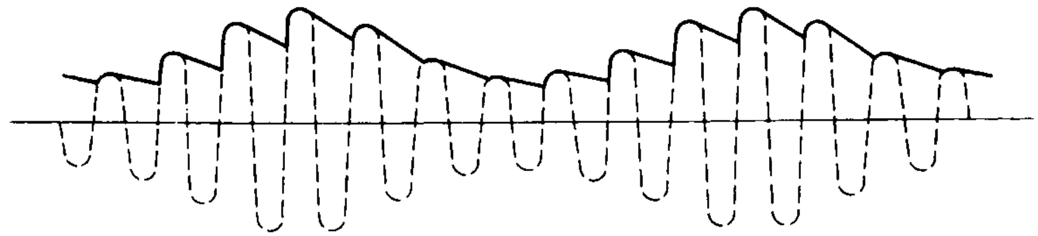


FIGURE 12.33
Envelope detector input (dashed line) and output waveforms.

- which illustrates the input and the output signal waveforms of a diode detector. As the input signal is applied, the capacitor charges up until the input waveform begins to decrease. At this time the diode becomes open-circuited and the capacitor discharges through the load resistance R_L as $V_L = V_p \exp(-t/R_L C)$ where V_p is the peak value of the input signal, and the diode opens at time t=0. The larger the value of capacitance used, the smaller will be the output ripple. However, C cannot be too large or it will not be able to follow the changes in the modulated signal. The time constant is often selected as $[(\omega_m \omega_c)^{-1}]^{1/2}$

Angle Modulation

- Information can also be transmitted by modulating the phase frequency. Angle modulation occupies a wider bandwidth, but it can provide better discrimination against noise and other interfering signals. An angle-modulated waveform can be written as $S(t) = A(t)\cos[\omega_c t + \theta(t)]$ where $\theta(t)$ representing the angle modulation. Angle modulation can be further subdivided into phase and frequency modulation, depending on whether it is the phase or the derivative of phase that is modulated. Frequency modulation and phase modulation are not distinct, since changing the frequency will result in a change in phase and modulating the phase also modulates the frequency.

Angle Modulators

- Frequency modulation can be achieved directly by modulating a VCO (direct FM) or indirectly by phase-modulating the RF waveform by the integrated audio input signal (indirect FM). Another method of FM is to use a phase-locked-loop as shown below

FM Demodulators

- The same type of circuitry is used for detecting both types of angle modulation, and we will refer to either process as FM detection. FM detectors are often referred to as frequency discriminators.
- The ideal FM detector produces an output voltage that changes linearly with changes in the input frequency as shown

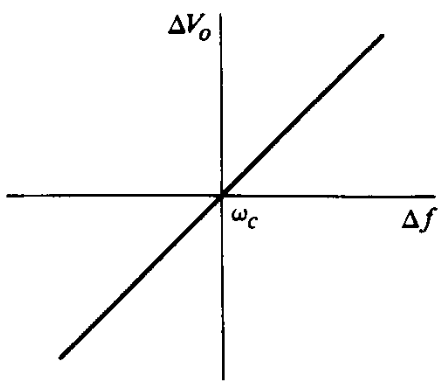


FIGURE 12.36
Ideal characteristics of a frequency-to-voltage converter.

- iation from the linear characteristic distorts the detected waveform. Amplitude modulation caused by noise can also cause distortion in the recovered signal. Limiting circuitry is usually included in FM detector to reduce the amount of amplitude modulation. The transfer characteristic of an ideal limiter is shown below

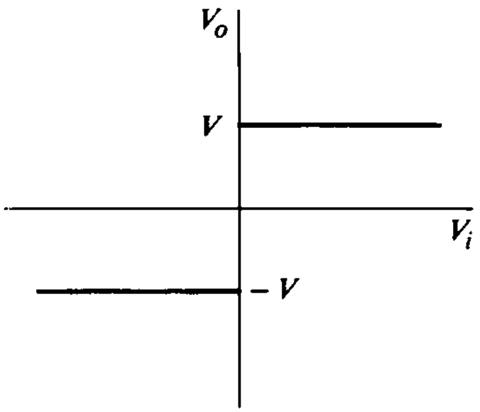


FIGURE 12.37
Transfer characteristics of an ideal limiter.

The limiter output is restricted to the values that depend only on the sign of the input. A single stage differential-pair limiter is shown

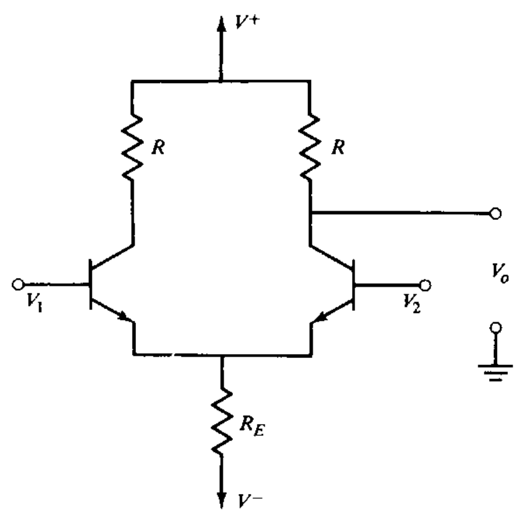


FIGURE 12.38
A differential-pair limiter.

- The circuit gives a close approximation to the ideal limiter characteristics. If the input signal is too small, several differential-pair stages may be cascaded in order for the output to be saturated. Integrated-circuit limiters frequently contain 3 cascaded stages.
- An analytical basis of FM detection is obtained by considering the derivative of the FM signal

$$\frac{d}{dt}\left\{A\cos[\omega_c t+\theta(t)]\right\} = -\left(\omega_c + \frac{d\theta}{dt}\right)A\sin[\omega_c t+\theta(t)]$$

- The derivative of an angle-modulated signal is an amplitude-modulated FM waveform. All the modulating information is contained in the amplitude of the differentiated waveform. Normally $\omega_c >> d\theta / dt$ if so the amplitude modulation can be removed with an envelope detector. The output of the envelope detector will be proportional to $\omega_c + d\theta / dt$, which is $\omega_c + KV_m(t)$ for a frequency-modulated waveform. If the output is then high-pass filtered to remove the constant term ω_c, the remainder will be proportional to the modulating signal. This technique has the disadvantage that any dc components in the modulating signal is lost.

- The magnitude of the frequency response of the parallel resonant circuit is shown below

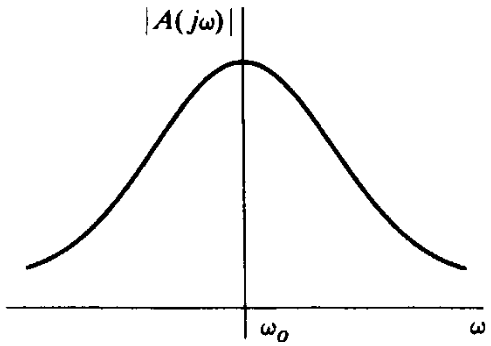


FIGURE 12.39
Tuned-circuit gain as a function of frequency.

- At frequency $\omega_c + \Delta\omega$,

$$|A(j\omega)| = \frac{R}{\left\{1 + Q^2[(\omega_c + \Delta\omega)/\omega_0 - \omega_0/(\omega_c + \Delta\omega]^2\right\}^{1/2}}$$

$$\approx \frac{R\omega_0(\Delta\omega + \omega_c)}{Q[\omega_0^2 - (\omega_c + \Delta\omega)^2]}$$

- provided ω_c is close enough to ω_0 so that

$$Q\left[\frac{\omega_c + \Delta\omega - \omega_0^2}{\omega_0(\omega_c + \Delta\omega)}\right] >> 1$$